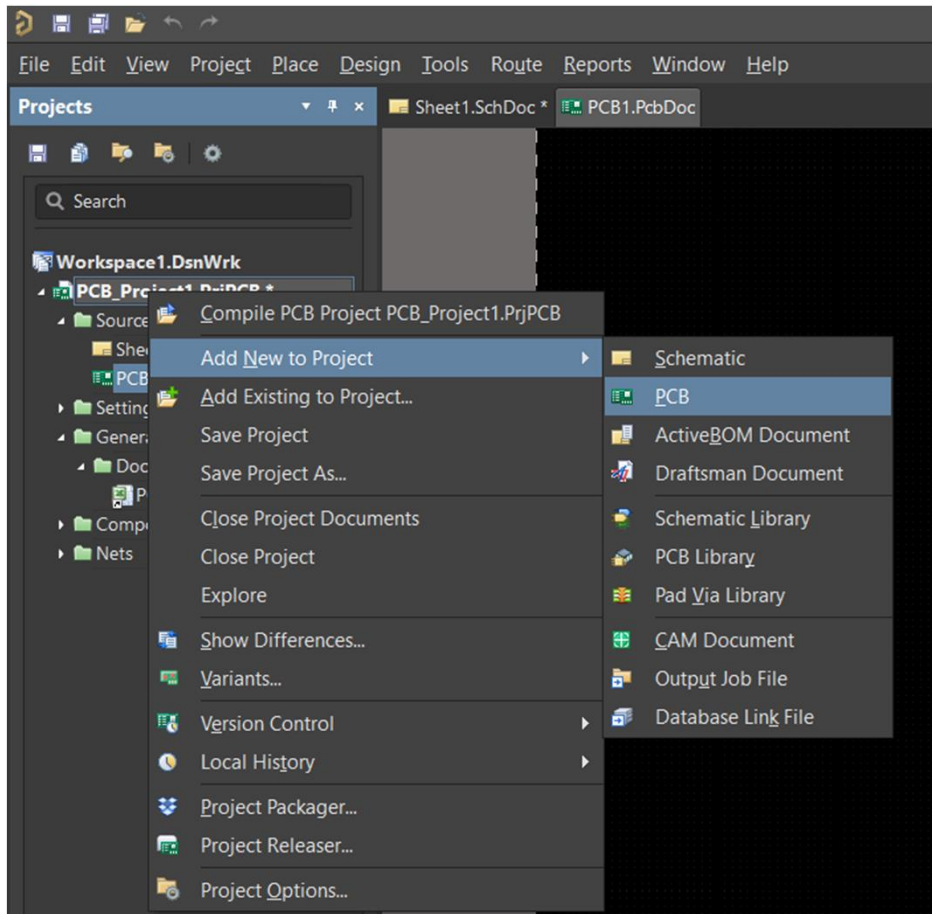


# Layout



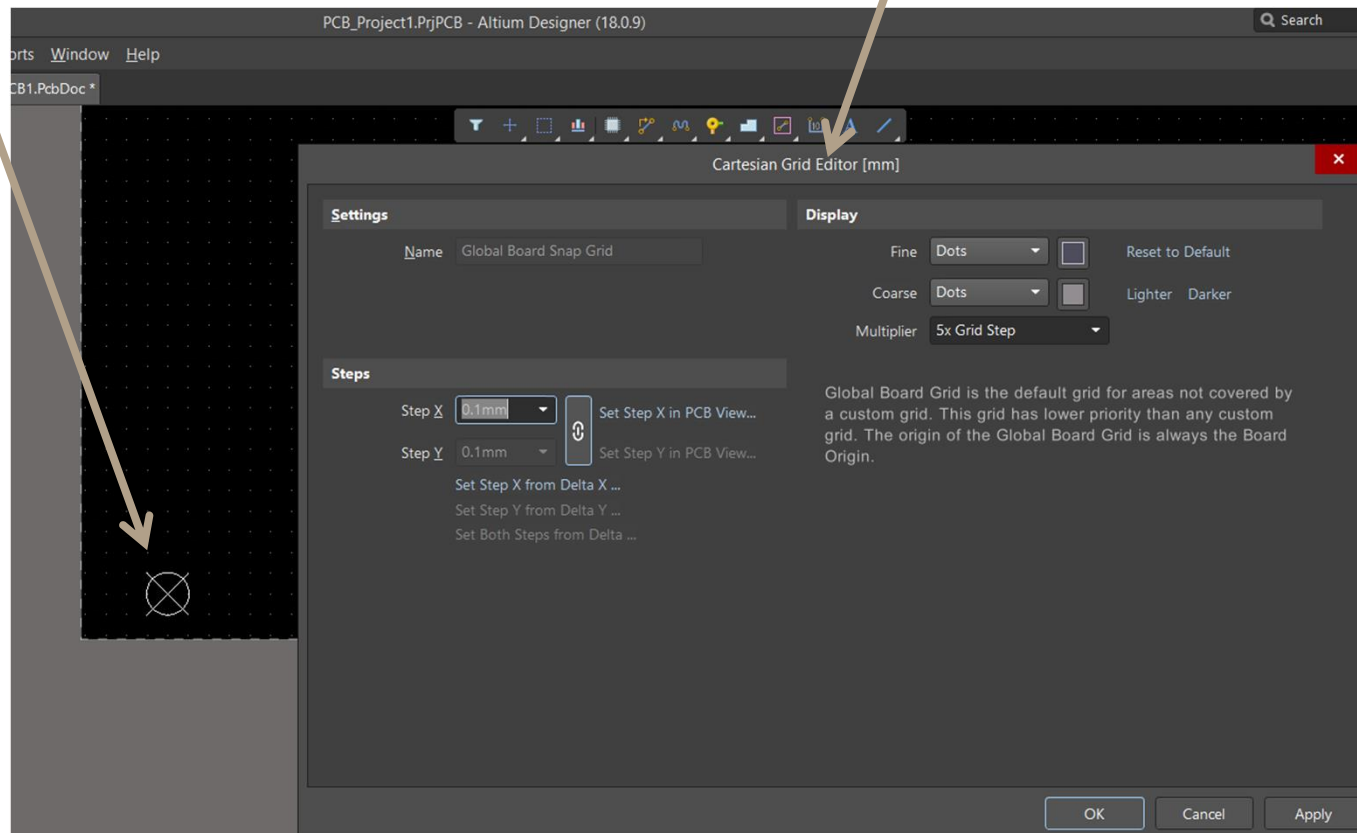
Attenzione all'unità di  
Misura e alla griglia

Ricordarsi di salvare il Documento per poter fare l'Update da schematico.

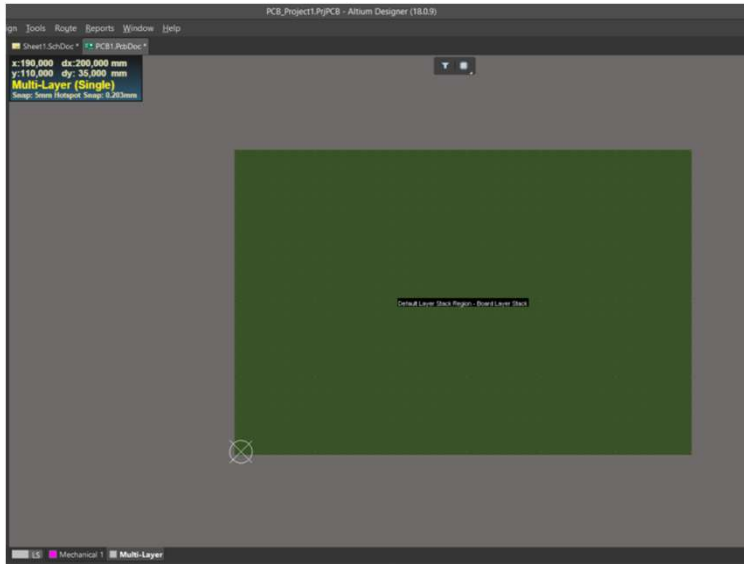
# Origine e Griglia

Edit – origin – set  
per spostare l'origine

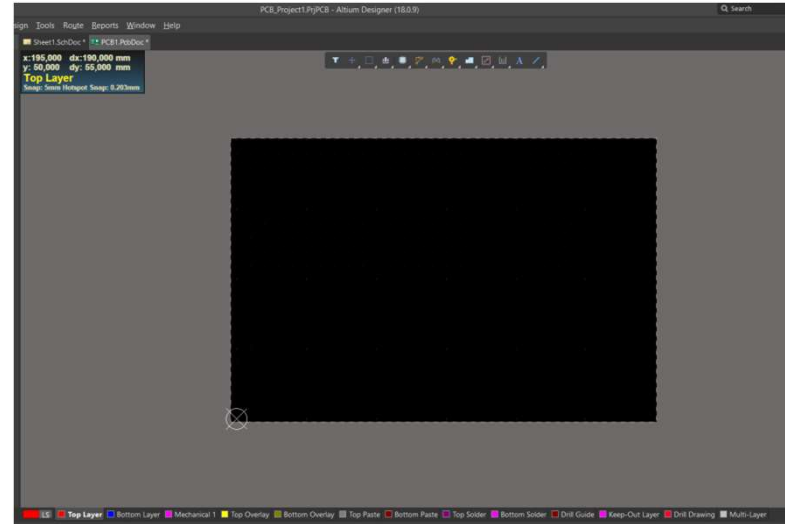
CTRL- G per impostare la griglia  
e per fare lo snap VIEW Grids Grids (V G G)



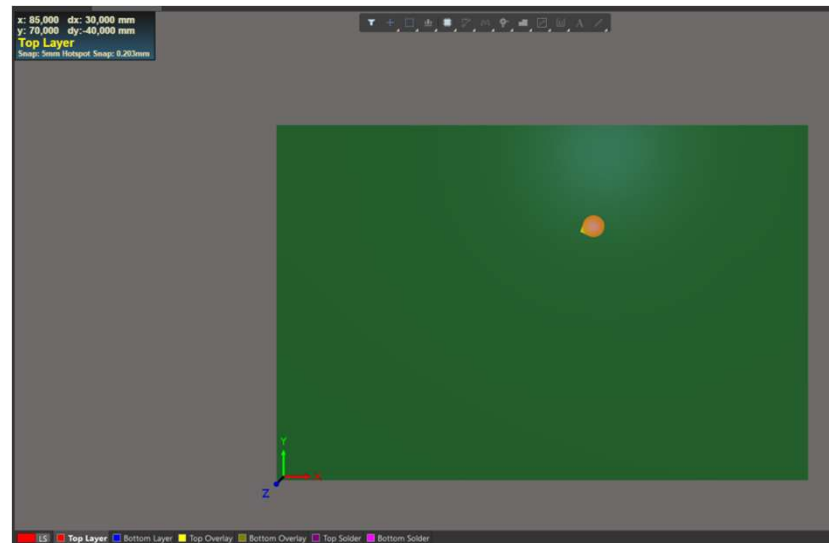
# Visualizzazione



'1' Board Planning Mode

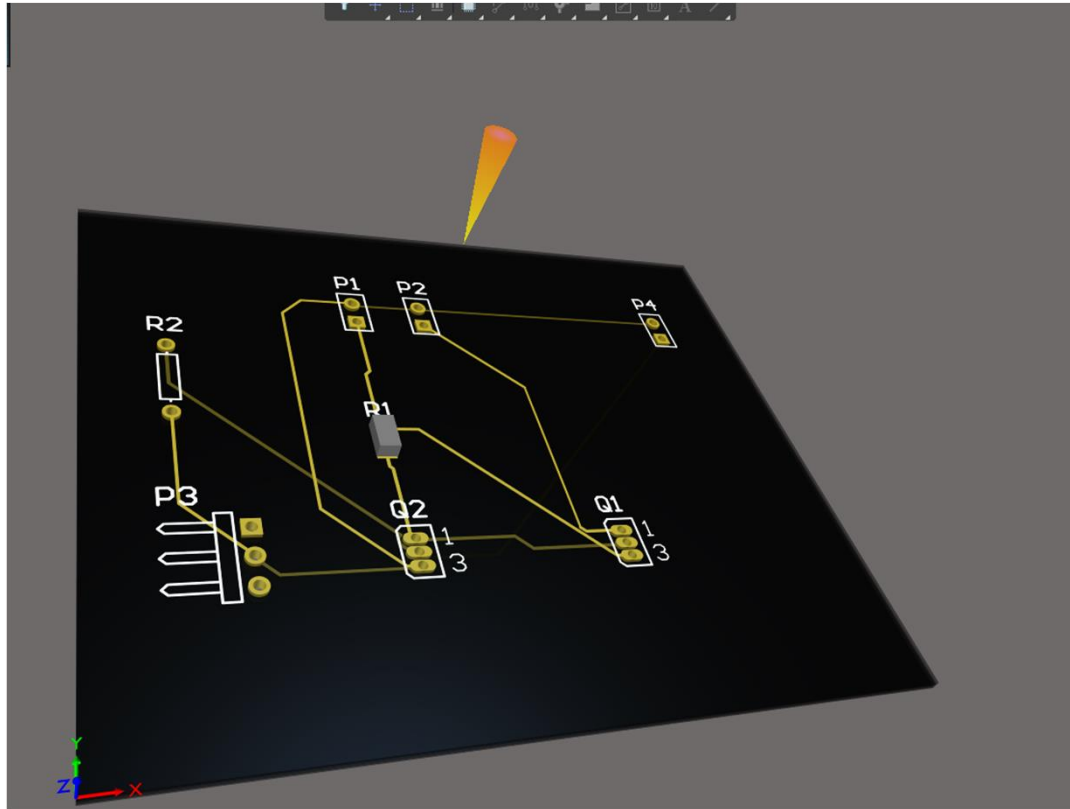


'2' 2D Layout Mode



'3' 3D Layout Mode

# 3D Layout Mode

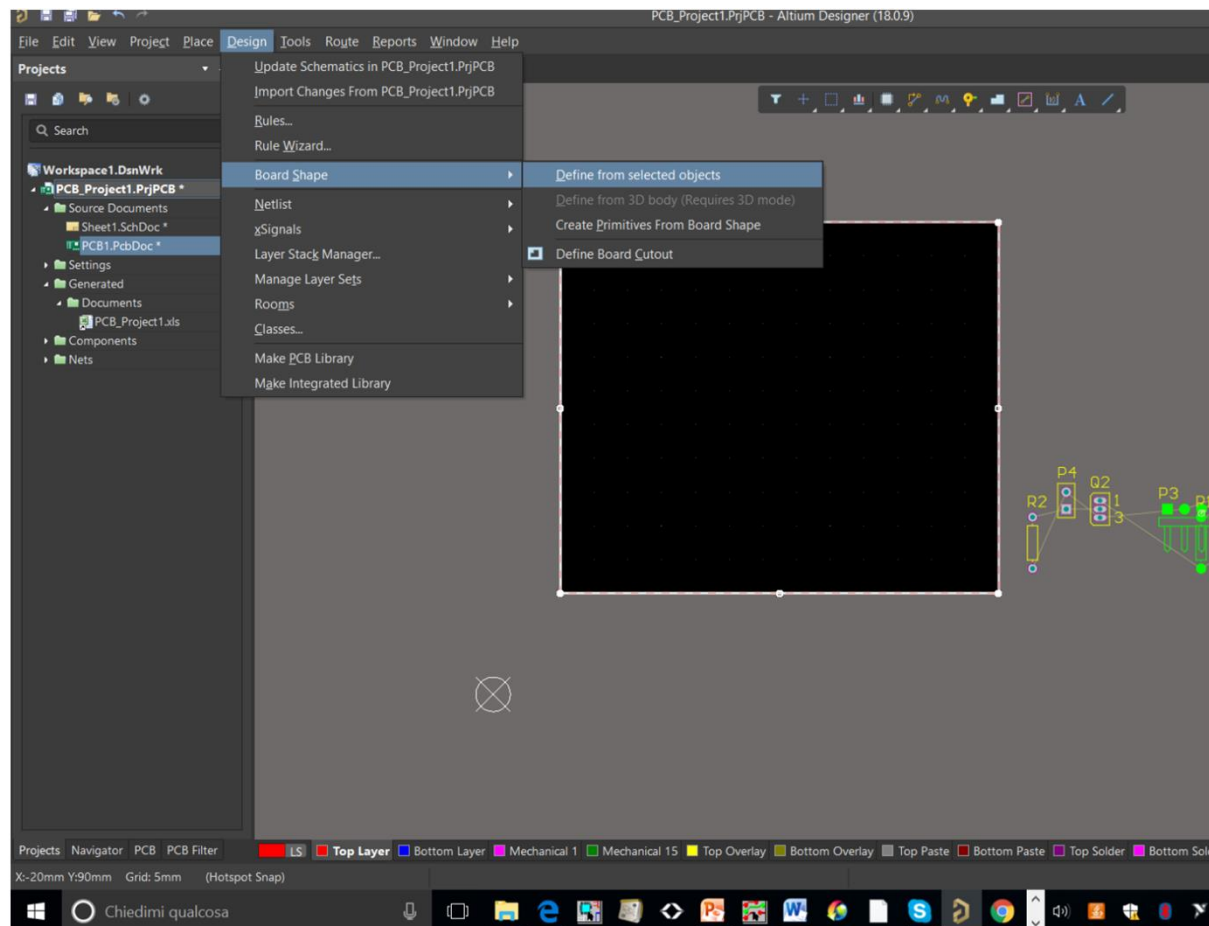


Right-drag Mouse  
Per spostare l'immagine

Shift+right-drag mouse  
Per ruotare la vista

# Board OutLine

1. Disegnare il contorno graficamente
2. Definirlo con DESIGN- BOARD SHAPE –DEFINE from selected object
3. Se necessario inserire dei CutOut

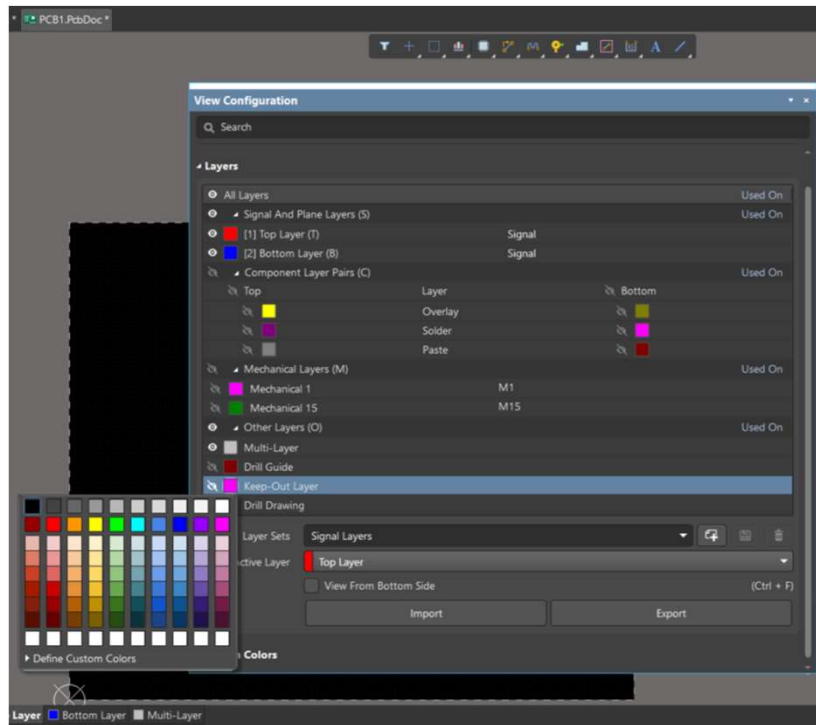


# Layers

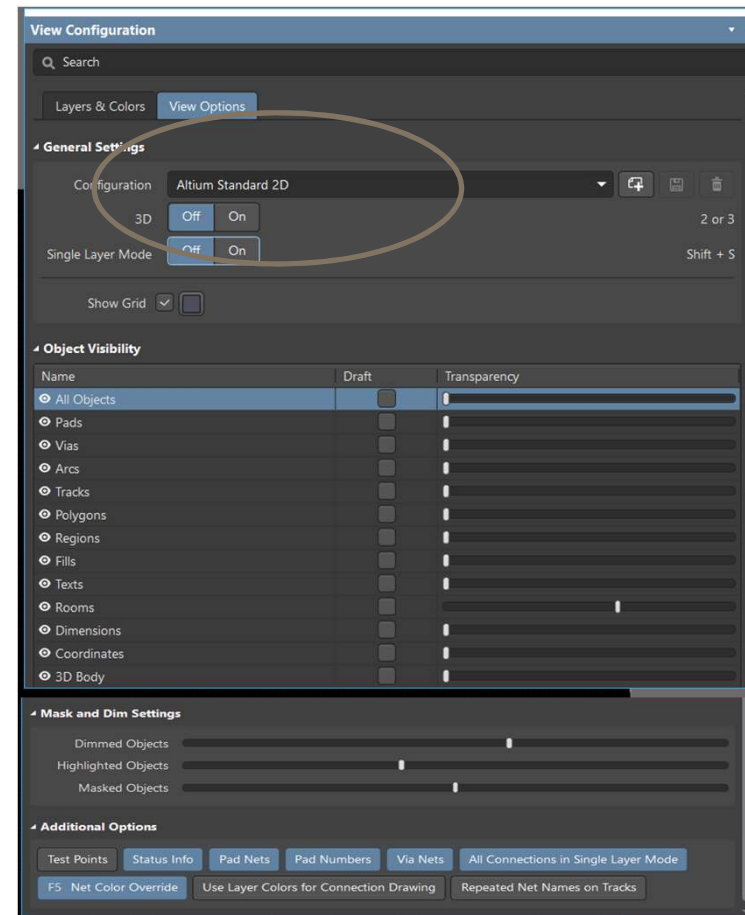
Elettrici: 32 + 16 interni di Powerplane

Meccanici: 32

Speciali: silkscreen, solder, paste, drill .....

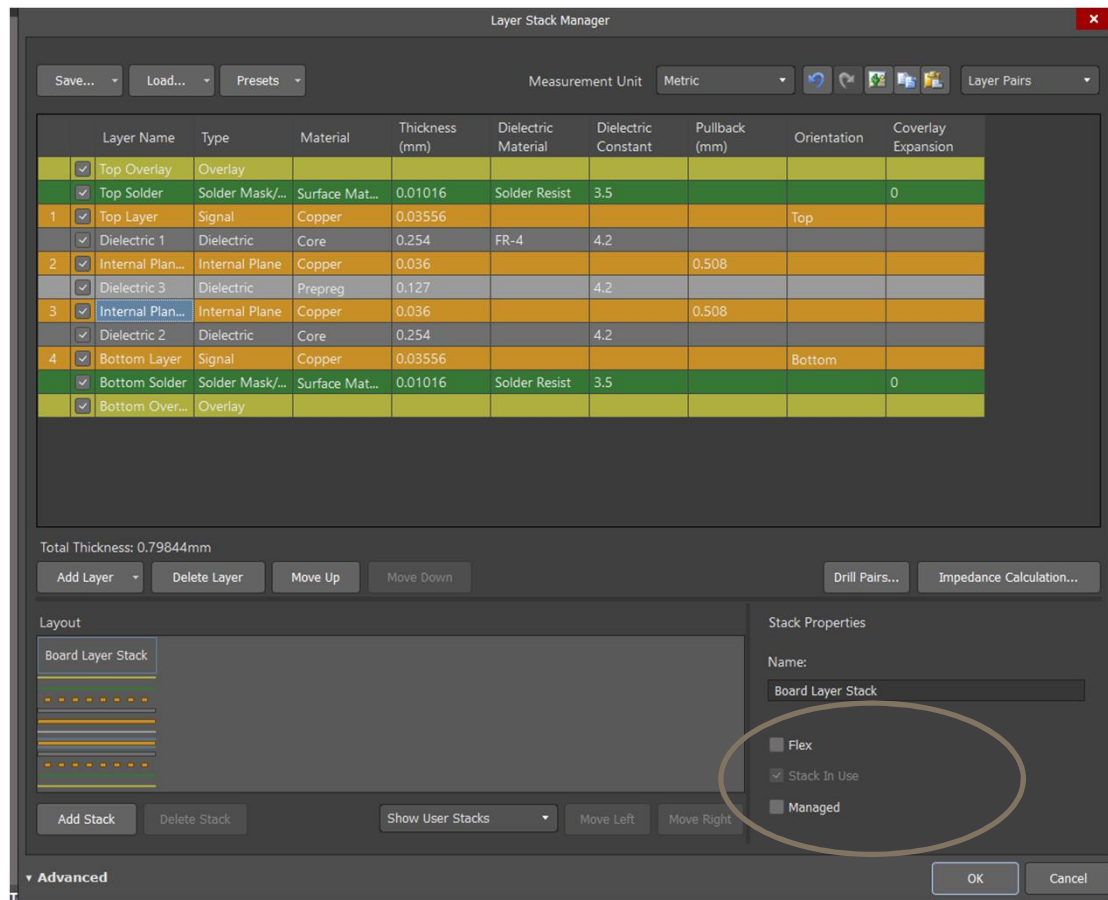


Per vedere la configurazione 'L'



# Layers stack manager

Si accede da Design – Layer Stack Manager



# Design Rules

The image shows two overlapping software windows from a PCB design application. The background window is the 'PCB Rules and Constraints Editor [mm]'. It features a tree view on the left with categories like 'Design Rules', 'Electrical', 'Routing', 'SMT', 'Mask', 'Planes', 'Testpoint', 'Manufacturing', 'High Speed', 'Placement', and 'Signal Integrity'. The 'Clearance' rule is selected under 'Electrical'. The main area shows configuration options for 'Where The First Object Matches' (All) and 'Where The Second Object Matches' (All). A diagram illustrates a track and a pad with a minimum clearance of 'N/A'. Below this is a table of constraints for various object types.

	Track	SMD Pad	TH Pad	Via	Copper	Text
Track	0.254					
SMD Pad	0.254	0.254				
TH Pad	0.254	0.254	0.254			
Via	0.254	0.254	0.254	0.254		
Copper	0.254	0.254	0.254	0.254	0.254	
Text	0.254	0.254	0.254	0.254	0.254	0.254
Hole	0	0	0	0	0	

The foreground window is the 'New Rule Wizard'. It prompts the user to 'Choose the Rule Type' and provides a list of options. The 'Name' field contains 'TEST'. The 'Electrical' category is expanded, showing sub-options: Clearance Constraint, Short-Circuit Constraint, Un-Routed Net Constraint, Un-Connected Pin Constraint, and Modified Polygon. The 'Routing' category is also expanded, showing: Width Constraint, Routing Topology, Routing Priority, Routing Layers, Routing Corners, Routing Via Style, Fanout Control, and Differential Pairs Routing. The 'SMT' category shows 'SMD To Corner Constraint'. Navigation buttons 'Cancel', 'Back', 'Next', and 'Finish' are at the bottom.



# Design Rules

- Rule Types:
  - Unary applicato all'oggetto ( es Width)
  - Binary fra oggetti ( esempio isolamento fra due oggetti)
- Rule Priority:
  - c'è un ordine di importanza nelle regole di disegno, quindi uso generale locale e specifico.

# New Rules

The screenshot displays the 'PCB Rules and Constraints Editor [mm]' window. A new rule named 'Width' is being configured. The 'Where The Object Matches' section is set to 'Custom Query' with the value 'InNet('GND')'. The 'Constraints' section shows 'Preferred Width' as 'N/A', 'Min Width' as 'N/A', and 'Max Width' as 'N/A'. A diagram of a yellow track is shown with width constraints. Below the diagram, there are checkboxes for 'Check Tracks/Arcs Min/Max Width Individually', 'Check Min/Max Width for Physically Connected Copper (tracks, arcs, fills, pads & vias)', 'Characteristic Impedance Driven Width', and 'Layers in layerstack only'. At the bottom, there is a table for 'Attributes on Layer'.

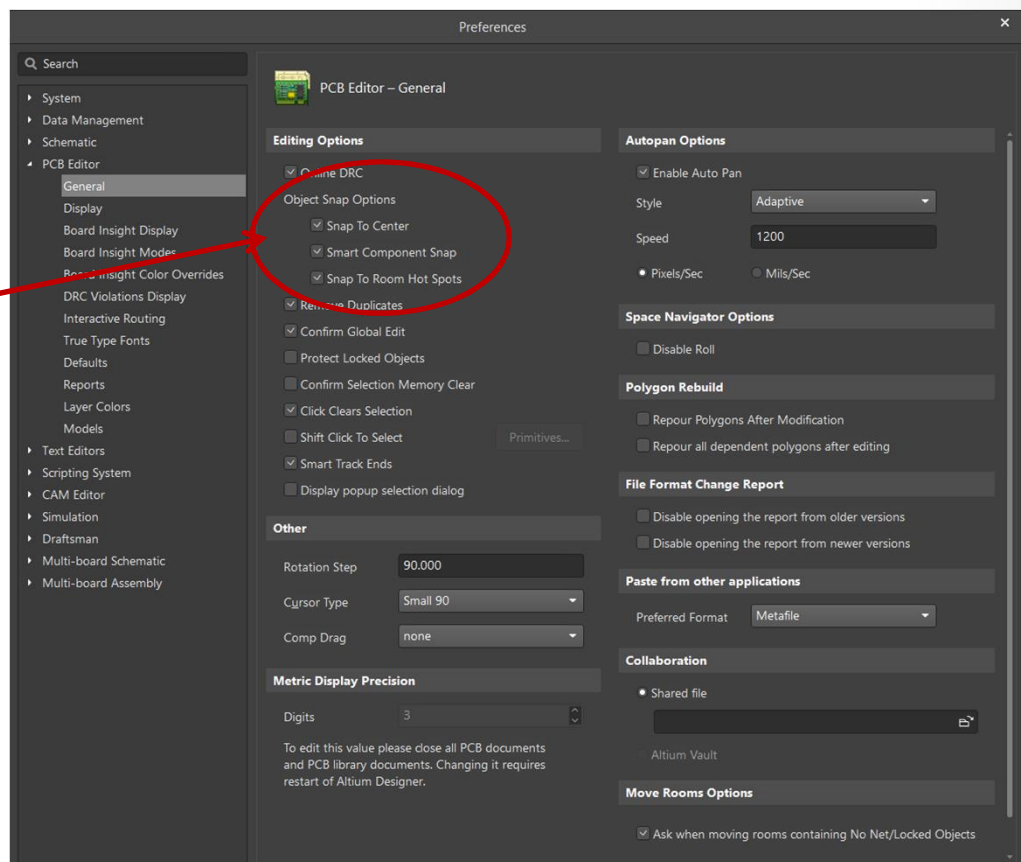
Attributes on Layer		Layer Stack Reference		Absolute Layer		
Min Width	Preferred Size	Max Width	Name	Index	Name	Index
0.1mm	0.3mm		3mm Top Layer	32	TopLayer	1
0.1mm	0.3mm		3mm Signal Layer 1	33	MidLayer1	2
0.1mm	0.3mm		3mm Bottom Layer	34	BottomLayer	32

# Posizionamento

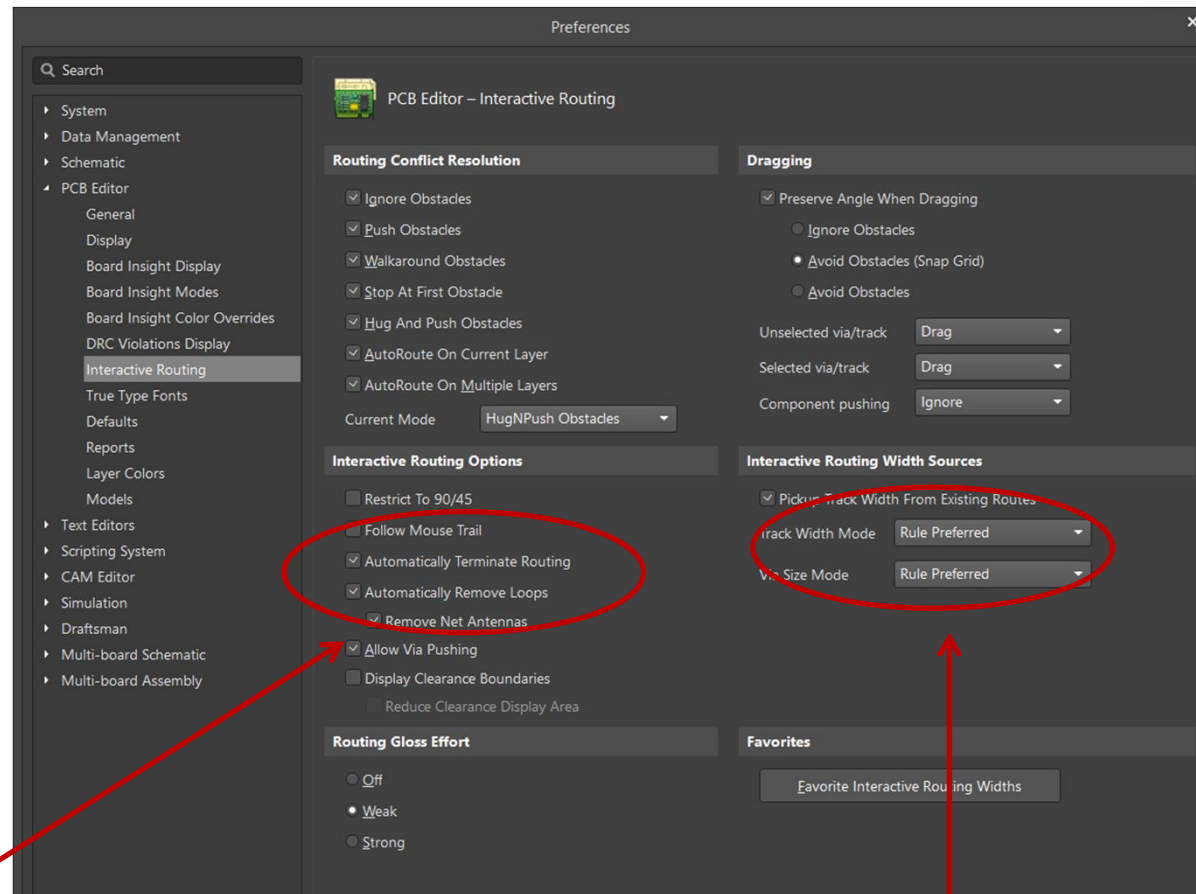
Snap to center mi garantisce che prendo dal centro il componente

Smart Component Snap lo prende dal pad più vicino

Posso disabilitare la visione delle Unconnected Net da View Connections



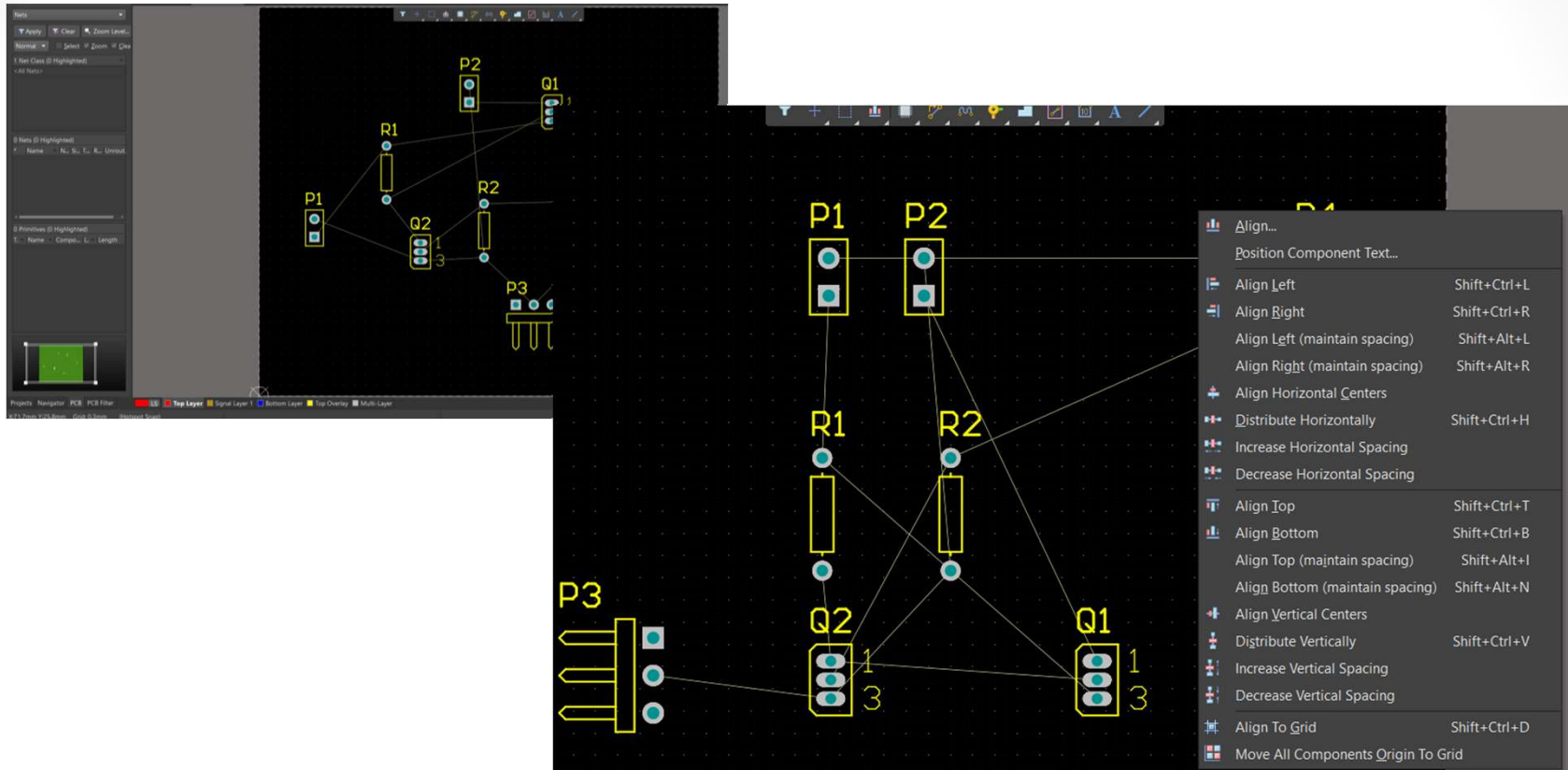
# Interactive Routing preferences



Termina in automatico la linea.  
El loop mi permette di cambiare  
la linea eliminando quello che è superfluo

Così usa le regole di preferenza  
per vias e wire

# Placement



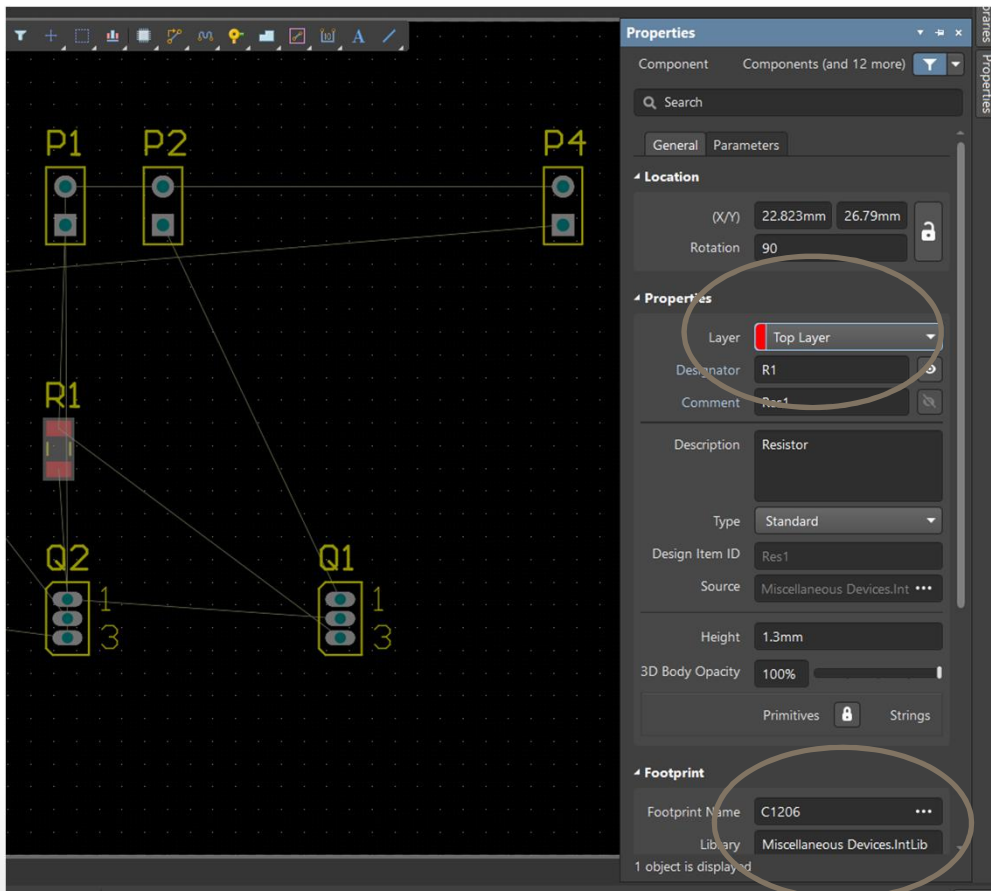
Spacebar per la rotazione.

Con Shift posso selezionare più parti e fare allineamenti con Align.

Posso muovere i componenti anche con le frecce tenendo CTRL.

# Footprint e Layer del componente

Doppio click sul componente e poi posso definire su che layer posizionarlo e cambiare la footprint -> facendo Update Schematic aggiorno lo schematico



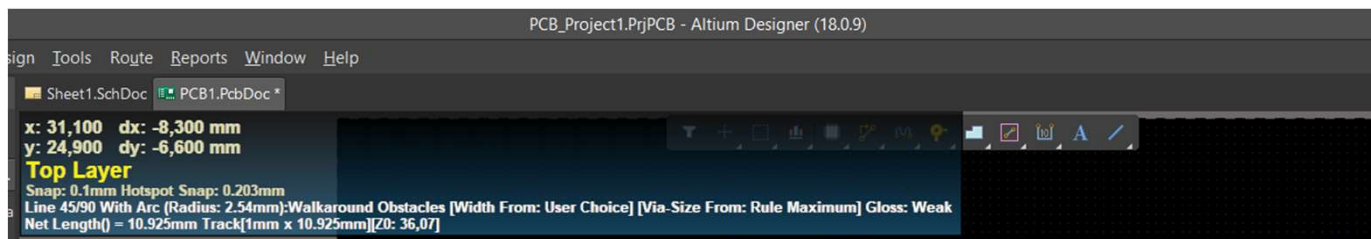
Per dove mettere i nomi (comment) :  
In PCB Editor – Default - Preferences comment o su ogni componente come parametro con doppio click

# Routing

- Shift+F1 per gli short cuts
- Chiusura in automatico di una pista con CTRL +LEFT Click
- U per unroute
- + per cambio layer generico
- \* per passare solo fra i layer di segnale
- Oppyure con ctrl+shift + roll
- Shift+W per dimensione pista
- Spacebar per flippare la pista
- Shift + Spacebar per cambiare l'angolo ( limitabile da PCB editor - Interactive Routing)
- Shift S per routing in singol layer e posso settare il modo in PCB-Editor Board Insight DIsplay

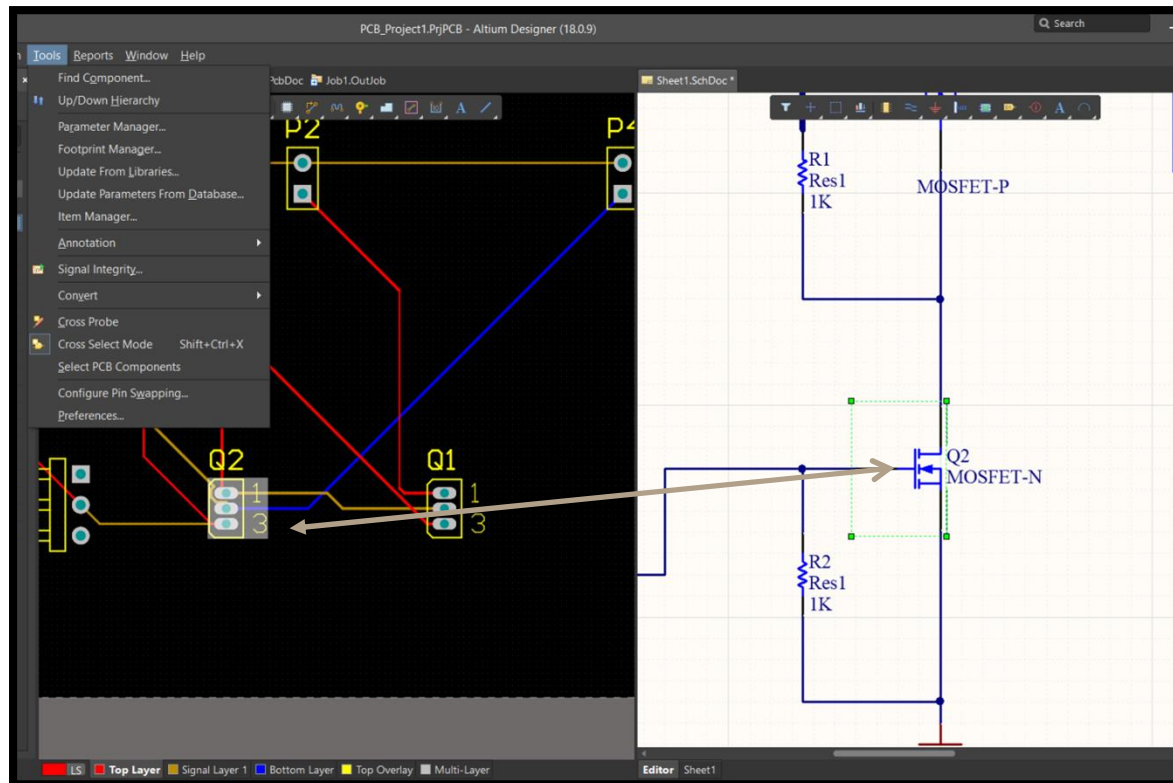
# Routing

- Shift+R per cambiare le modalità
  - Ignore: pista dove voglio
  - Stop at first obstacle
  - WALKAROUND giro intorno
  - Push riposiziona i componenti ch esi possono muovere senza dare errori
  - Hug&Push unione di walkaround e Push
  - Autoroute in current layer
  - Autoroute ion Multipler layer





# Cross Selector Mode



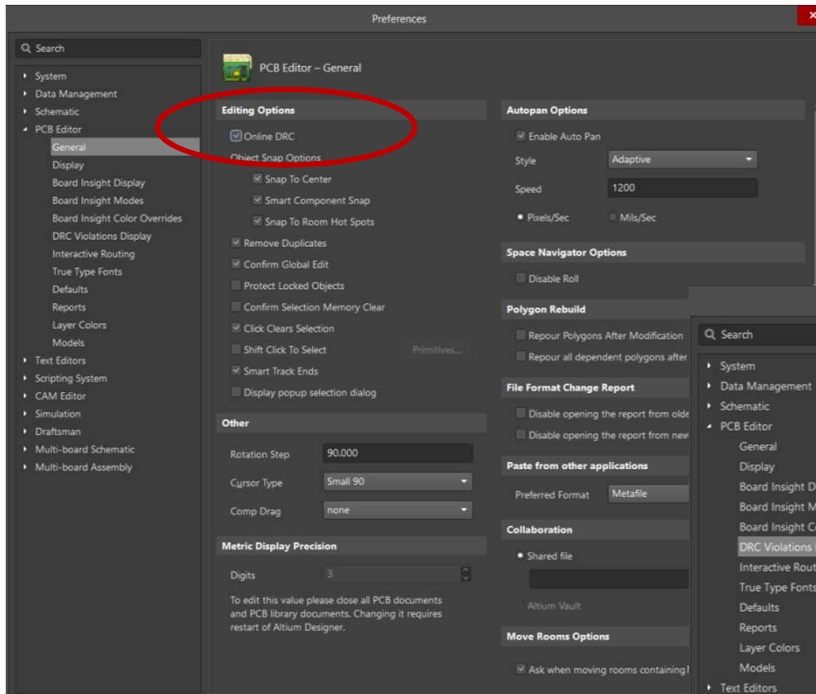
Lo attivo da Tools e deve esserlo sia per layout che per schematico

# Autorouting

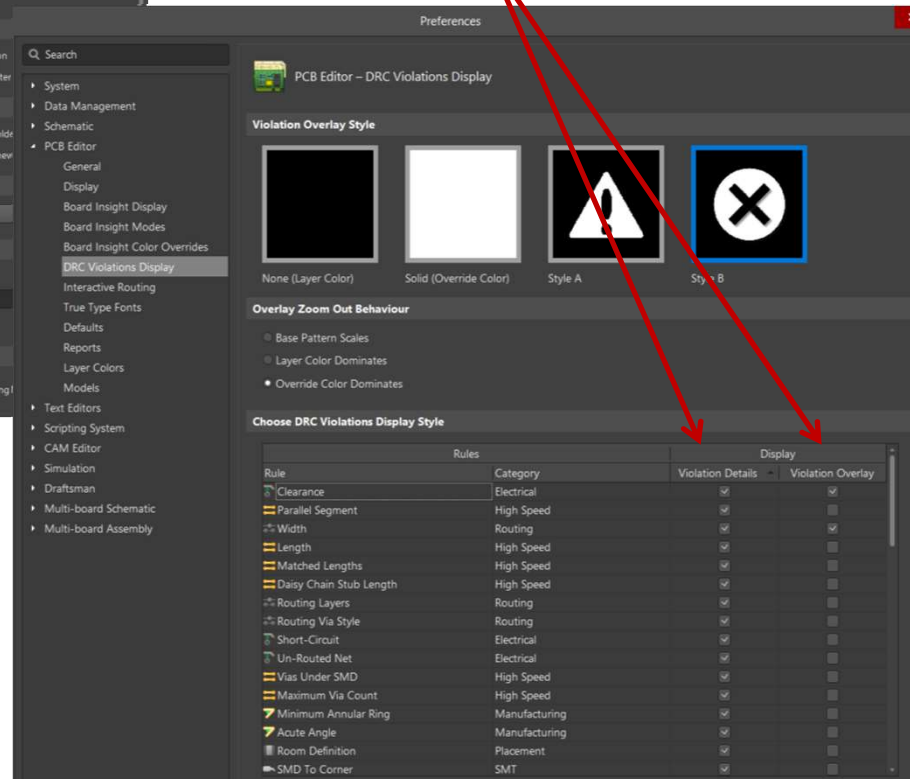
The screenshot shows the Altium Designer interface for PCB Project1.PrjPCB (18.0.9). The 'Route' menu is open, with 'Auto Route' selected. The 'Routing Setup Report' dialog is open, showing 'Errors and Warnings - 0 Errors 0 Warnings 1 Hint'. The 'Layer Directions' dialog is also open, showing a table of layer settings.

Layer	Current Setting	Actual Direction
Top Layer	Automatic	Vertical
Signal Layer 1	Automatic	4 o'clock
Bottom Layer	Automatic	2 o'clock

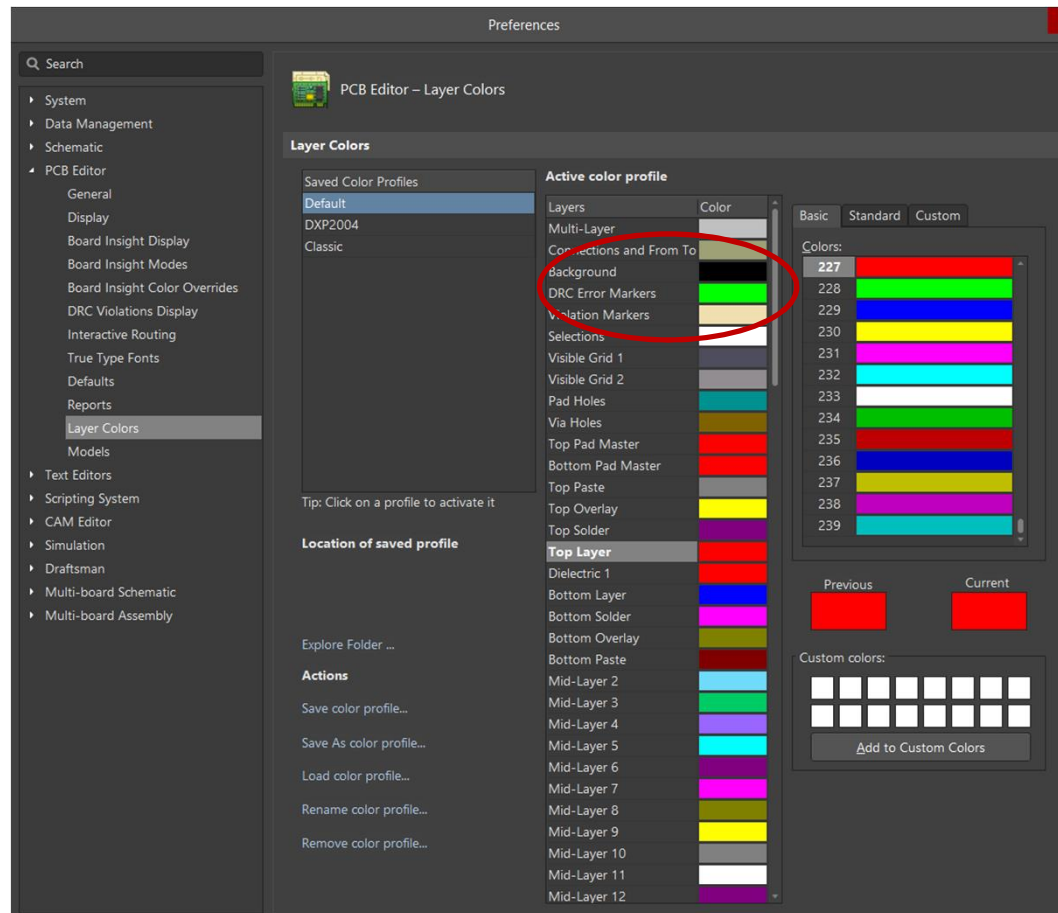
# VERIFY



Il DRC può essere attivo Online  
e le verifiche possono essere  
attivate o meno



# Verify



# Verify – Tools DRC

Design Rule Checker [mm]

Report Options

Rules To Check

- Electrical
- Routing
- SMT
- Testpoint
- Manufacturing
- High Speed
- Placement
- Signal Integrity

DRC Report Options

- Create Report File
- Create Violations
- Sub-Net Details
- Verify Shorting Copper
- Report Drilled SMT Pads
- Report Multilayer Pads with 0 size Hole

Stop when 500 violations found

DRC Report Options

- Report Broken Planes
- Report Dead Copper larger than 0.065 sq. mm
- Report Starved Thermals with less than 50%

NOTE: To generate Report File you must save your PCB document first. To speed the process of rule checking enable only the rules that are required. Note: Options are only enabled when corresponding rules have On-line DRC tests for design rule violations as you work. Include a Design dialog to be able to test for a particular rule type.

Run Design Rule Check... OK Cancel

Rule	Category	Online	Batch
Clearance	Electrical	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Modified Polygon	Electrical	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Short-Circuit	Electrical	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Un-Connected Pin	Electrical	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Un-Routed Net	Electrical	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Sempre

Solo quando faccio il DRC

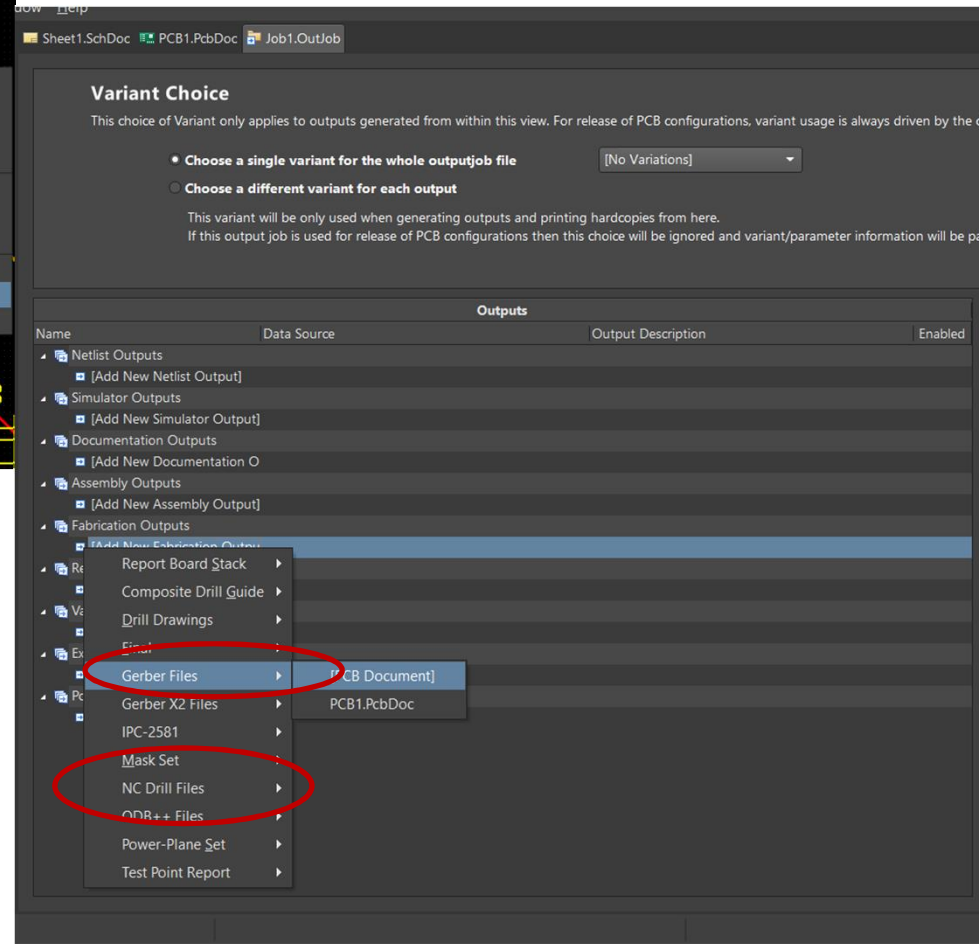
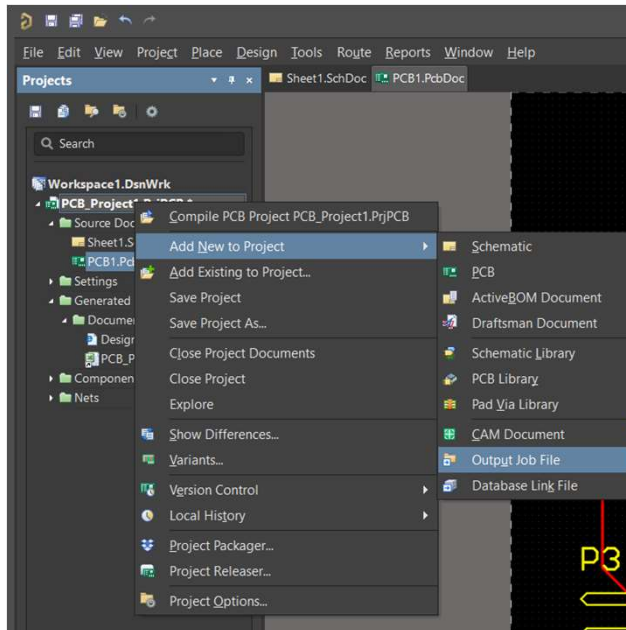
# Verify – DRC messages

The screenshot displays the Altium Designer 18.0.9 interface. The top window shows a list of DRC messages with columns for Class, Document, Source, Message, Time, Date, and No. Below this, the 'Design Rule Verification Report' is open, showing a table of rule violations.

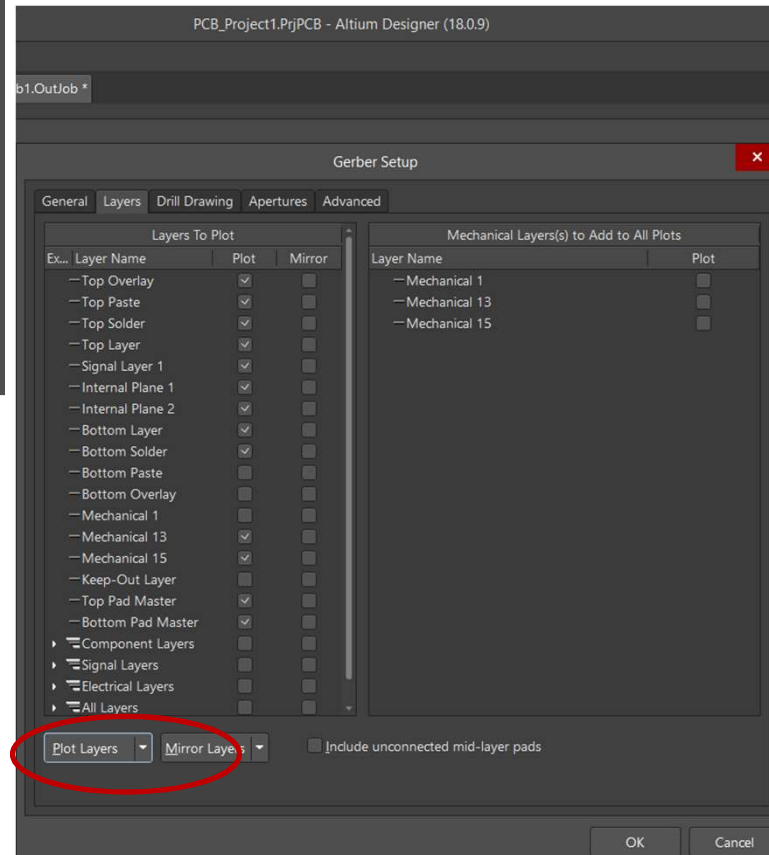
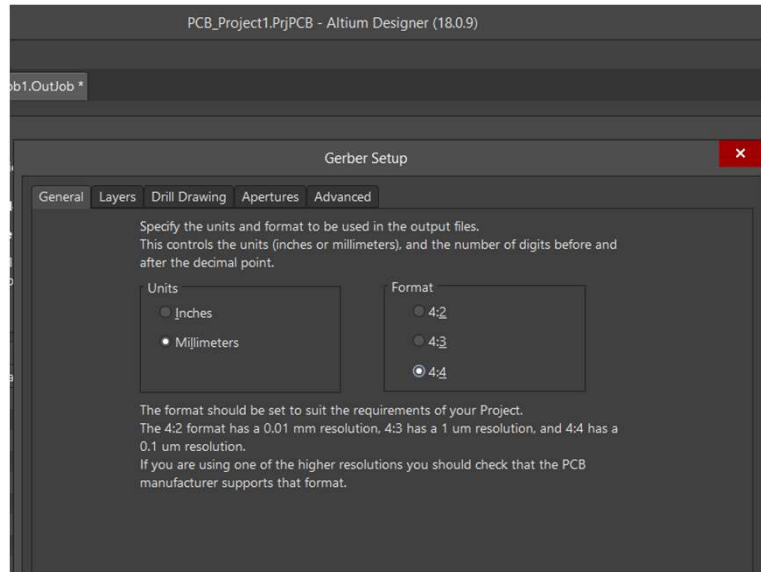
Rule Violations	Count
Clearance Constraint (Gap=0.1mm) (All) (All)	1
Short-Circuit Constraint (Allowed=No) (All) (All)	1
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No) (Allow shelved: No)	0
Width Constraint (Min=0.25mm) (Max=0.5mm) (Preferred=0.254mm) (InNet(GND))	0
Width Constraint (Min=0.1mm) (Max=3mm) (Preferred=0.3mm) (All)	1
Power Plane Connect Rule(Relief_Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air_Gap=0.254mm) (Entries=4) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All) (All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All) (All)	4
Silk To Solder Mask (Clearance=0.254mm) (IsPad) (All)	2
Silk to Silk (Clearance=0.254mm) (All) (All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
<b>Total</b>	<b>9</b>

# OUTPUT

Creare un file output-job e salvarlo



# GERBER



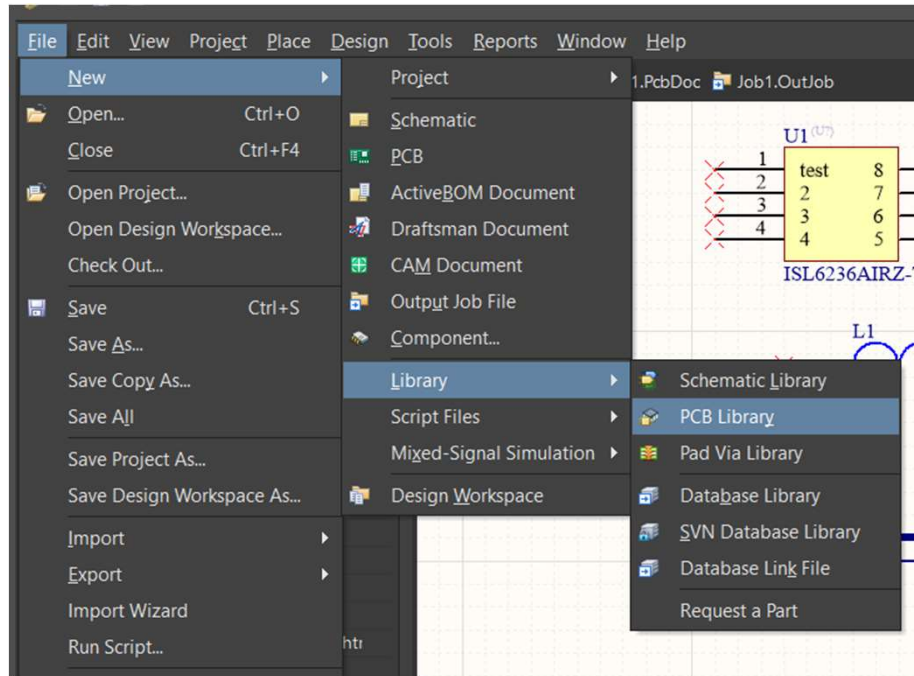


# Nc drill e pick and place

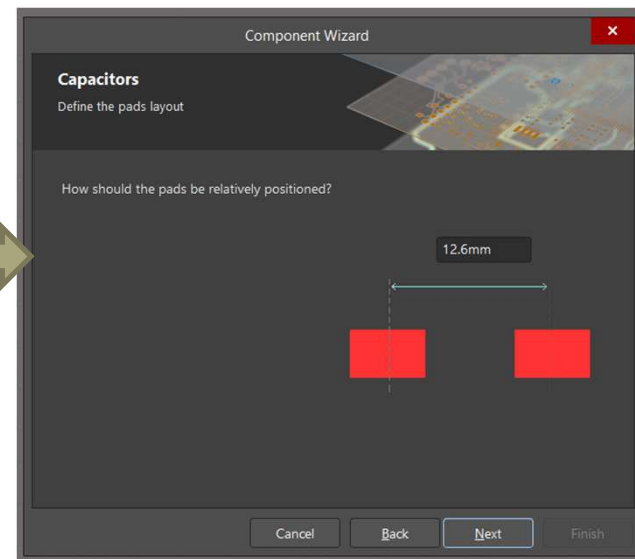
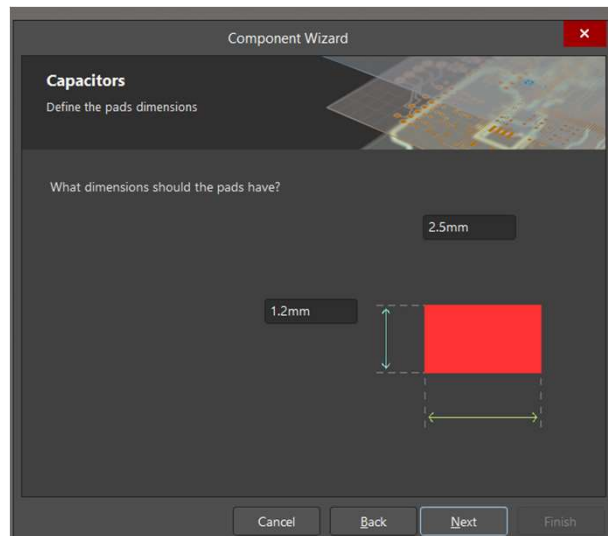
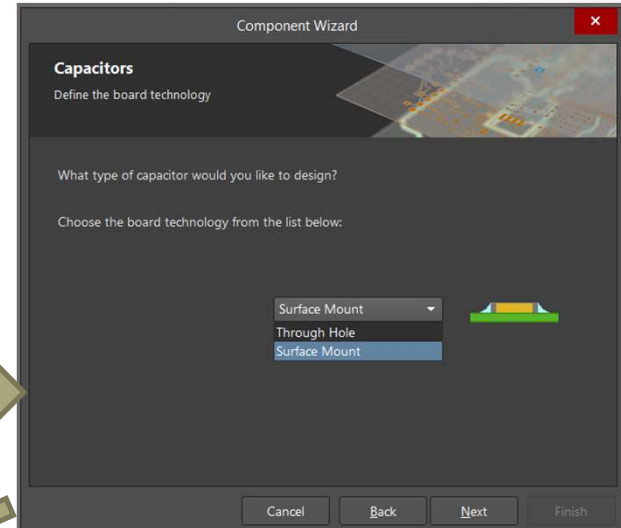
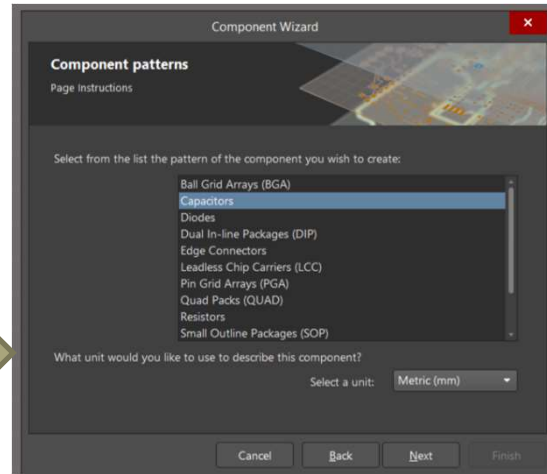
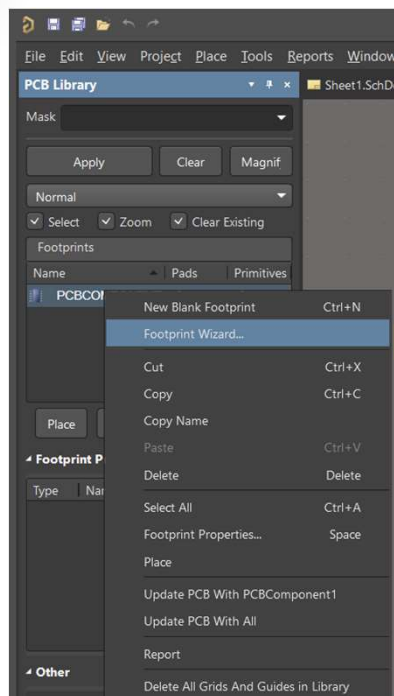
The image shows two dialog boxes from Altium Designer (18.0.9) for PCB Project1.PrjPCB. The 'NC Drill Setup' dialog is on the left, and the 'Pick and Place Setup' dialog is on the right. The 'Pick and Place Setup' dialog features a table with the following data:

Designator	Comment	Layer	Footprint	Center-X(mil)	Center-Y(mil)	Rotation	Description
R2	Res1	TopLayer	AXIAL-0.3	259.842	1322.834	90	Resistor
R1	Res1	TopLayer	C1206	898.542	1054.725	90	Resistor
Q2	MOSFET-N	TopLayer	E3	921.260	614.174	0	N-Chann
Q1	MOSFET-P	TopLayer	E3	1629.922	614.174	0	P-Chann
P4	Header 2	TopLayer	HDR1X2	2208.662	1686.220	90	Header, 2
P3	Header 3H	TopLayer	HDR1X3H	448.818	625.984	270	Header, 3
P2	Header 2	TopLayer	HDR1X2	1169.292	1686.220	90	Header, 2
P1	Header 2	TopLayer	HDR1X2	915.748	1686.220	90	Header, 2

# New FootPrint

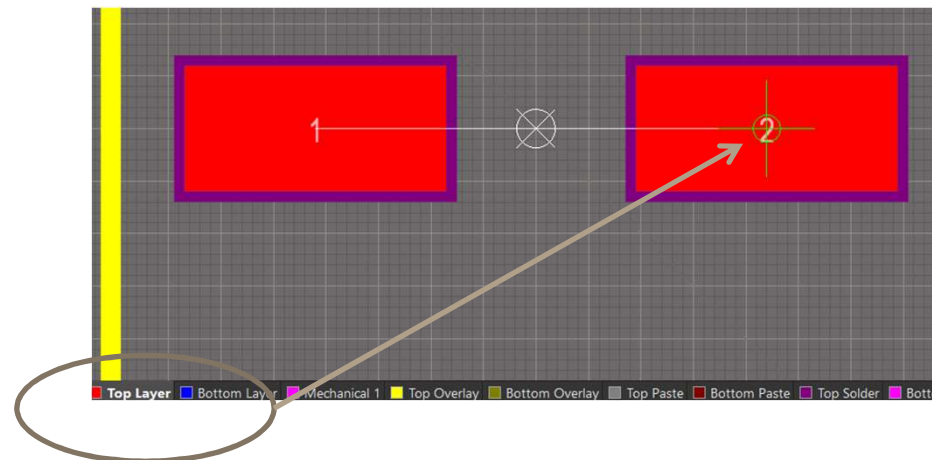
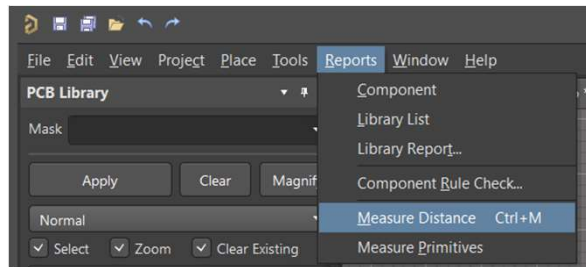


# Footprint Wizard



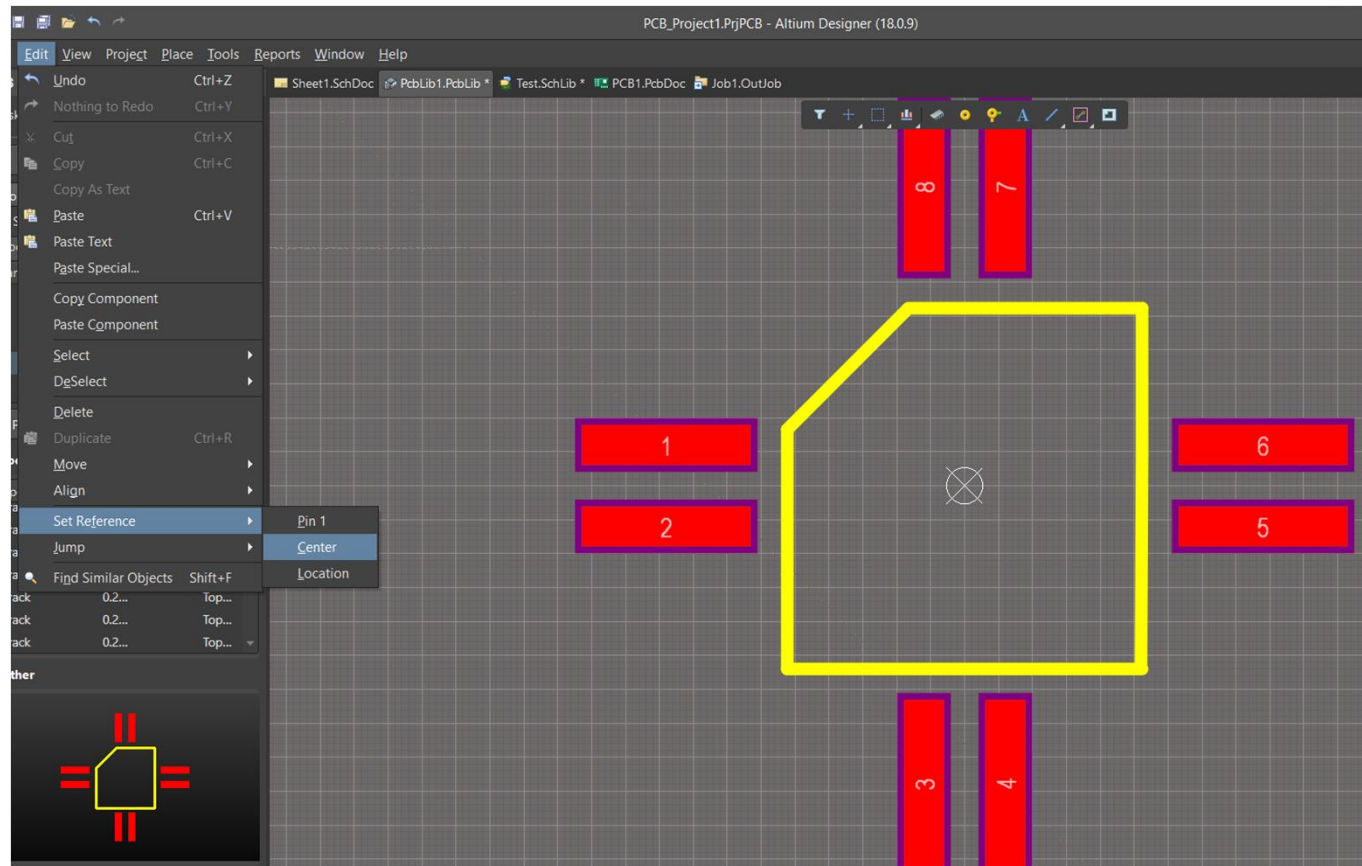
# New Footprint

Attenzione alla griglia: anche se ho scelto Metric ho lo schermo in Inch.  
Lo cambio con Ctrl +G



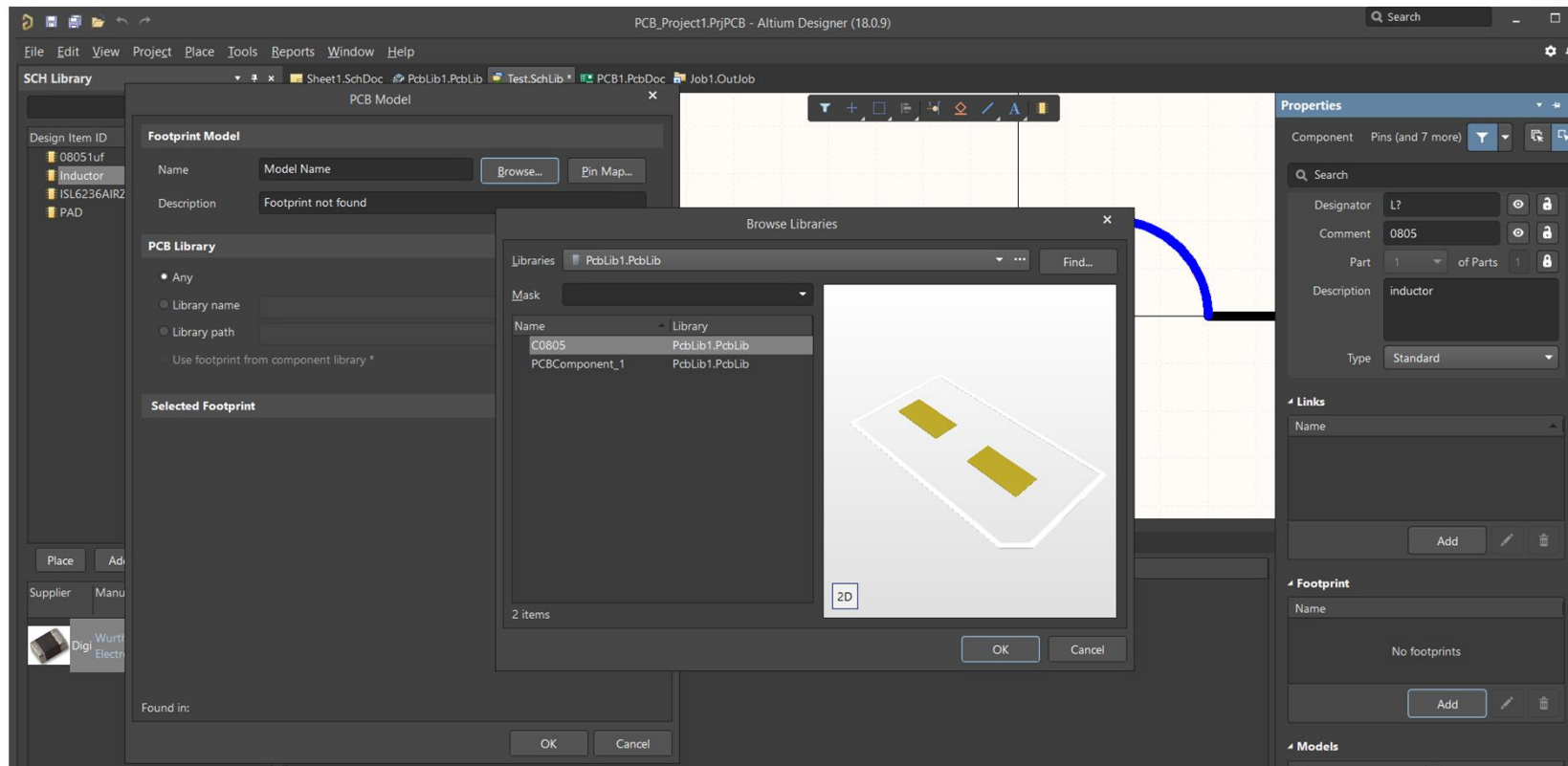
Misurare le distanze : ideale essere sul layer di interesse  
Per pulire Shift+C

# Reference Point

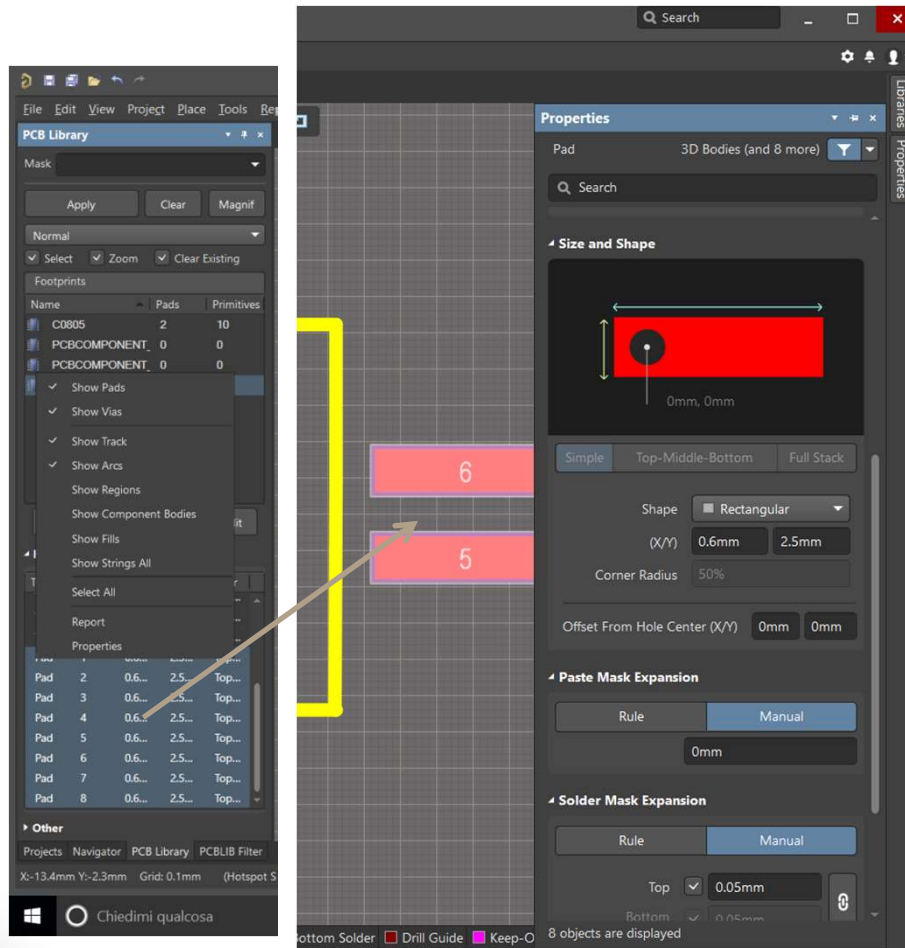


# Associazione con Schematico

Da SCH Library ---properties del componente e poi add



# Proprietà dei PAD



Nota: attenzione ai fori plated o no

Il nome del PAD deve corrispondere con quello nello schematico

# Esempio/ Esercizio

Realizzare il PCB dello schematico di esempio, realizzando una nuova libreria dei componenti.

