### Layout



#### Attenzione all'unità di Misura e alla griglia

Ricordarsi di salvare il Documento pe rpoter fare l'Update da schematico.



Progettazione PCB 31/05/2018

#### Visualizzazione



"1' Board Planning Mode



#### '2' 2D Layout Mode

'3' 3D Layout Mode



Progettazione PCB 31/05/2018

#### 3D Layout Mode



Right-drag Mouse Per spostare l'immagine

Shift+right-drag mouse Per ruotare la vista

# 31/05/2018

#### **Board OutLine**

- 1. Disegnare il contorno graficamente
- 2. Definirlo con DESIGN- BOARD SHAPE DEFINE from selected object
- 3. Se necessario inserire dei CutOut

3 = a		PCB_Project1.PrjPCB - Altium Designer (18.0.9)
<u>File Edit View Project Place</u>	esign <u>T</u> ools Ro <u>u</u> te <u>R</u> eports <u>W</u> indow <u>H</u> elp	
Projects •	Update Schematics in PCB_Project1.PrjPCB	
	Import Changes From PCB_Project1.PrjPCB	T + T + T M T M A /
	<u>R</u> ules	
C Search	Rule <u>W</u> izard	
🕼 Workspace 1. Dsn Wrk	Board Shape	Define from selected objects
PCB_Project1.PrjPCB *	Netlict	Define from 3D body (Requires 3D mode)
Sheet1.SchDoc *	vSignale	Create Primitives From Board Shape
PCB1.PcbDoc *	Laver Stack Manager	
End Settings	Manago Lavor Sotr	
Generated      Documents	Pooms	
PCB_Project1.ds		
Components		
🕨 🧰 Nets	Make PCB Library	
	Make Integrated Library	
		•
		02 P3
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Projects Navigator PCB PCB Filter	LS 🔲 Top Layer 📃 Bottom Layer 📃 Me	echanical 1 🔲 Mechanical 15 📕 Top Overlay 📕 Bottom Overlay 📕 Top Paste 📕 Bottom Paste 🔲 Top Solder 📕 Bottom Sold
X:-20mm Y:90mm Grid: 5mm (Hots	pot Snap)	
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CB1.PdbDoc *				
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	[2] Bottom Laver (B)	Sign		
	Component Laver Pairs	s (C)		Used On
	a Top		Rottom	
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	× 1	Solder	× -	
	a 🗖	Paste		
a	<ul> <li>Mechanical Layers (M)</li> </ul>			
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8 100 100 100 100 100 100 100 100 100 10	Mechanical 15			
•	<ul> <li>Other Layers (O)</li> </ul>			
•	Multi-Layer			
<u>8</u>	Drill Guide			
	Keep-Out Layer			
	Drill Drawing			
	Layer Sets Signal La	iyers		4 🗉 🕯
	ctive Layer Top Lay	yer		
	View I	From Bottom Side		
		Import		
Define Custom Colors	Colors			
XX				

Per vedere la configurazione 'L'

Elettrici: 32 + 16 interni di Powerplane Meccanici: 32 Speciali: silkscreen, solder, paste, drill .....



#### Layers stack manager

#### Si accede da Design – Layer Stack Manager

Layer Stack Manager									×			
Sa	ve	← Load				Measure	ment Unit Me	etric	• 🧐 🥙 💆	1 🗈 🛍	Layer Pairs	
		Layer Name	Туре	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation	Coverlay Expansion		
			Overlay									
		Top Solder	Solder Mask/	Surface Mat		Solder Resist	3.5					
1			Signal	Copper	0.03556				Тор			
				Core	0.254		4.2					
2			Internal Plane	Copper	0.036			0.508				
			Dielectric	Prepreg	0.127		4.2					
3		Internal Plan		Copper	0.036			0.508				
				Core	0.254		4.2					
4			Signal	Copper	0.03556				Bottom			
		Bottom Solder	Solder Mask/	Surface Mat		Solder Resist	3.5					
		Bottom Over	Overlay									
-												
Total	Thic	kness: 0.79844r										
Ac	d Lay	yer - Del	ete Layer	Move Up					Drill Pair	s Imp	bedance Calculation	
Layo	ut								Stack Properties			
Boar	rd Lay	ver Stack							Name:			
									Board Laver Stack			
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A	ld Sta	ack Deleti			Show User Stack			love Right				
* Adva	nce	d										ncol
Auva	mee											ncer

#### Design Rules



#### Design Rules

• Rule Types:

Unary applicato all'oggetto ( es Width) Binary fra oggetti ( esempio isolamento fra due oggetti)

• Rule Priority:

c'è un ordine di importanza nelle regole di disegno, quindi uso generale locale e specifico.

#### **New Rules**



#### Posizionamento

Q Sea

Simu
Draft
Multi Multi

Snap to center mi garantisce che prendo dal centro il componente

Smart Component Snap lo prende dal pad più vicino

Posso disabilitare la visione delle Unconnected Net da View Connections

	Preference			
nagement	PCB Editor – General			
c Editing	g Options	Autopan Options		
c Free Colors Colors Colors Colors Colors Colors Colors Colors Color Colors Col	y options Same DRC set Snap Options Sanap To Center Sanar Component Snap Sanar Component Snap Sanar Component Snap Sanar Component Snap Sonfirm Global Edit rrotect Locked Objects Sconfirm Selection Memory Clear Tick Clears Selection hift Click To Select mart Track Ends Neplay popup selection dialog		Adaptive	
Other		Disable opening	the report from newer versions	
ard Schematic Rota ard Assembly Cyrs Com	tion Step 90.000 for Type Small 90 hp Drag none	Paste from other ap	pplications Metafile <del>•</del>	
Motrie	n Display Precision	Collaboration		
Digit To e and resta	ts 3 dit this value please close all PCB docum PCB library documents. Changing it requ art of Altium Designer.	Shared file     S ents Altium Vault irres     Move Rooms Option	ns	

# Interactive Routing preferences

	Preferences	×
Q Search  System  Data Management	PCB Editor – Interactive Routing	
Schematic	Routing Conflict Resolution	Dragging
PCB Editor     General     Display     Board Insight Display     Board Insight Display     Board Insight Modes     Board Insight Color Overrides     DRC Violations Display     Interactive Routing     True Type Fonts     Defaults	<ul> <li>✓ Ignore Obstacles</li> <li>✓ Push Obstacles</li> <li>✓ Walkaround Obstacles</li> <li>✓ Stop At First Obstacle</li> <li>✓ Hug And Push Obstacles</li> <li>✓ AutoRoute On Current Layer</li> <li>✓ AutoRoute On Multiple Layers</li> <li>Current Mode</li> </ul>	<ul> <li>Preserve Angle When Dragging         <ul> <li>Ignore Obstacles</li> <li>Avoid Obstacles (Snap Grid)</li> <li>Avoid Obstacles</li> </ul> </li> <li>Unselected via/track Drag          <ul> <li>Selected via/track Drag</li> <li>Component pushing Ignore</li> <li>Ignore</li> </ul> </li> </ul>
Reports	Interactive Routing Options	Interactive Routing Width Sources
Models • Text Editors • Scripting System • CAM Editor • Simulation • Draftsman • Multi-board Schematic • Multi-board Assembly	Restrict To 90/45 Follow Mouse Trail Automatically Terminate Routing Automatically Remove Loops Remove Net Antennas Allow Via Pushing Display Clearance Boundaries	<ul> <li>✓ Pider Track Width From Existing Routes</li> <li>Track Width Mode Rule Preferred</li> <li>Vis Size Mode Rule Preferred</li> </ul>
	Reduce Clearance Display Area Routing Gloss Effort      Qff      Weak      Strong	Favorites <u>Favorite Interactive Rou</u> ing Widths

Termina in automatico la linea. Ell loop mi permette di cambiare la linea eliminando quello che è superfluo

Così usa le regole di preferenza per vias e wire

#### Placement



Spacebar per la rotazione.

Con Shift posso selezionare più parti e fare allineamenti con Align. Posso muovere i componenti anche con le frecce tenendo CTRL.

#### Footprint e Layer del componente

Doppio click sul componente e poi posso definire su che layer posizionarlo e cambiare la footprint -→ facendo Update Schematic aggiorno lo schematico



Per dove mettere i nomi (comment) : In PCB Editor – Default -Preferences comment o su ogni componente come parametro con doppio click

# Progettazione PCB 31/05/2018

#### Routing

- Shift+F1 per gli short cuts
- Chiusura in automatico di una pista con CTRL +LEFT Click
- U per unroute
- + per cambio layer generico
- \* per passare solo fra i layer di segnale
- Oppyure con ctrl+shift + roll
- Shift+W per dimensione pista
- Spacebar per flippare la pista
- Shift + Spacebar per cambiare l'angolo (limitabile da PCB editor - Interactive Routing)
- Shift S per routing in singol layer e posso settare il modo in PCB-Editor Board Insight DIsplay

# Routing

• Shift+R per cambiare le modalità

- Ignore: pista dove voglio
- Stop at first obstacle
- WALKAROUND giro intorno
- Push riposiziona i componenti ch esi possono muovere senza dare errori
- Hug&Push unione di walkaround e Push
- Autoroute in current layer
- Autoroute ion Multipler layer



#### **Cross Selector Mode**



Lo attivo da Tools e deve esserlo sia per layout che per schematico

#### Autorouting



#### VERIFY

		Preferences			
L Search System Data Management	PCB Editor	– General			
Schematic	Editing Options		Autopan Options		
PCB Editor	🖸 Online DRC		🗑 Enable Auto Pa		
Display	Object Snap Option				
Board Insight Display			Frank	1200	
Board Insight Modes		ponent Snap	opeeu	1200	
Board Insight Color Overrides			<ul> <li>Pixels/Sec</li> </ul>		
DRC Violations Display	Remove Duplica				
Interactive Routing	Confirm Global	Edit	Space Navigator C	ptions	
Defaults	Protect Locked	Objects			
Reports	Confirm Selectio	on Memory Clear	Polygon Rebuild		
	Click Clears Sele	ction			-
Models	Shift Click To Sel	lect Primitives	Repour Polygo	ns After Modification	4 3
	Smart Track End		Repour all depe	endent polygons after	
Scripting System	Display popup s	election dialog	File Format Change	e Report	• Da
Simulation			Disable openin	a the report from olde	
Draftsman	Other		Disable openin	the report from pay	
Multi-board Schematic	Rotation Step	90.000			
Multi-board Assembly			Paste from other a	pplications	
	Cursor Type	Small 90 👻	Preferred Format		
			Collaboration		
	Metric Display Prec	ision	<ul> <li>Shared file</li> </ul>		
	Digits				
	To edit this value p	lease dose all PCB documents			
	and PCB library do				
	restart of Album D	esigner.	Move Rooms Opti	ons	
			M Ask when movi	ng rooms containing l	
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#### Il DRC può essere attivo Online e le verifiche possono essere attivate o meno

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PCB Editor – DRC Violations Display Violation Overlay Style  None (Layer Color) Solid (Override Color) Solid (Over	PCB Editor – DRC Violations D	lisplay	
Violation Overlay Style  Violation Overlay Style  None (Layer Color) Solid (Override Color) Solid (Overide Color) Solid (Override Color)	on Overlay Style		
None (Layer Color)       Solid (Override Color)       Style A       Style A         None (Layer Color)       Solid (Override Color)       Style A       Style A         Style A       Style A       Style A       Style A         Base Pattern Scales       Layer Color Dominates       Style A       Style A         • Override Color Dominates       • Override Color Dominates       Style A       Style A         • Override Color Dominates       • Override Color Dominates       Style A       Style A         • Override Color Dominates       • Override Color Dominates       • Override Color Dominates         • Override Color Dominates       • Override Color Dominates       • Override Color Dominates         • Override Color Dominates       • Override Color Dominates       • Override Color Dominates         • Override Color Dominates       • Override Color Dominates       • Override Color Dominates         • Override Color Dominates       • Override Color Dominates       • Override Color Dominates         • Override Color Dominates       • Override Color Dominates       • Override Color Dominates         • Override Color Dominates       • Override Color Dominates       • Override Color Dominates         • Override Color Dominates       • Override Color Dominates       • Override Color Dominates         • Override Color Dominates			
Overlay Zoom Out Behaviour <ul> <li>Base Pattern Scales</li> <li>Layer Color Dominates</li> <li>Override Color Dominates</li> <li>Override Color Dominates</li> <li>Decise DRC Violations Display Style</li> <li>Rules</li> <li>Category</li> <li>Violation Details</li> <li>Violation Details</li></ul>	e (Layer Color) Solid (Over	ride Color) Style A	
Base Pattern Scales     Layer Color Dominates     Override Color Dominates Choose DRC Violations Display Style     Rules     Rules     Category Violation Details Violation Vio	v Zoom Out Behaviour		
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# Verify

	Prefer	ences			×
Q Search					
<ul> <li>System</li> </ul>	PCB Editor – Layer Colors				
<ul> <li>Data Management</li> </ul>					
Schematic	Layer Colors				
PCB Editor		Active color profile			
General	Saved Color Profiles	Active color profile			
Display	Default	Layers	Color	Basic Standard	Custom
Board Insight Display	DXP2004	Multi-Layer			
Board Insight Modes	Classic	Contractions and From To		Colors:	
Board Insight Color Operator		Background		227	
DBC Malating Diala		DRC Error Markers		220	
DRC Violations Display		Violation Markers		229	
Interactive Routing		Selections		230	
True Type Fonts		Visible Grid 1		231	
Defaults		Visible Grid 2	<u> </u>	232	
Reports		Pad Holes		233	
Layer Colors		Via Holes		234	
Models		Top Pad Master		235	
Text Editors		Bottom Pad Master		237	
Scripting System	Tip: Click on a profile to activate it	Top Paste	_	238	
CAM Editor		Top Overlay		239	
Simulation	Location of saved profile	Top Solder		233	2
Draftsman		Top Layer			
Multi-hoard Schematic		Dielectric 1		Previous	Current
Multi-board Scientatic		Bottom Layer			
<ul> <li>Multi-board Assembly</li> </ul>		Bottom Solder			
	Explore Folder	Bottom Overlay		Custom colors:	
	Actions	Mid Lawor 2		custoin colors.	
		Mid Layer 2			
	Save color profile	Mid-Layer J	_		
	Save As color profile	Mid-Layer 5	_	Add to (	Curtom Colors
		Mid-Laver 6		Mad to t	Lusion Colors
	Load color profile	Mid-Layer 7			
	Rename color profile	Mid-Laver 8			
		Mid-Laver 9			
		Mid-Laver 10			
		Mid-Laver 11			
		Mid-Laver 12			

### Verify – Tools DRC

Report Options     Rules To Check     Reles To Check     Control     Retrical     SMT     Testpoint     Munufacturing     High Speed     Placement     Signal Integrity	Design Rule Checker [mm] DRC Report Options Create Report Elle Create Violations Sub-Net Details Verify Shorting Copper Report Drilled SMT Parts Report Duilled SMT Parts Report Multilayer Parts with 0 size Hole Stop when 500 violations four	nd	×		Sempre	
	DRC Report Options				Altuin Designer (16.0.5)	
	🗹 Report Broken Planes			Design	Rule Checker [mm]	
	Report Dead Copper larger than	0.065 sq. mm	Report Options	Rule	Category	Online Batch
	Report Starved Thermals with less than	50% av	a Rules To Check	Clearance	Electrical	N N
	NOTE: To generate Report File you must save	e your PCB document first.	a Electrical	Modified Polygon Short-Circuit	Electrical	2 2 2
	To speed the process of rule checking enable performed. Note: Options are only enabled	only the rules that are required when corresponding rules h	Ji SMT	Tun-Connected Pin	Electrical	N N
	On-line DRC tests for design rule violations a dialog to be able to test for a particular rule	as you work. Include a Desig type.	gr ✓ lestpoint Manufacturing ➡ High Speed ■ Placement Isignal Integrity	ੌ Un-Routed Net	Electrical	7
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#### Verify – DRC messages

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Eile View Project Window Help			¢ # 1 -
Messages			
Class         Document         Source         Message           Class         Document         Clarance Constraint - PCB1 PdbDoc         Advanced PCB         Clarance Constraint: (Collision < 0.1mm) Between Track (26.178mm.28.14mm)(39.988mm.14.33mm) on Top Layer And Track (37.684mm.17.276mm)(37.684mm.33.576m           Il [Short-Grouit Constraint Volta PCB1 PdbDoc         Advanced PCB         Short-Grouit Constraint: Track (37.684mm.17.276mm)(37.684mm.33.576mm) on Top Layer And Track (37.684mm.17.276mm)(37.684mm.33.576mm)           IV Width Constraint Volta PCB1 PdbDoc         Advanced PCB         Width Constraint: Track (37.684mm.17.276mm)(37.684mm.33.576mm) on Top Layer Actual Width = Smm, Target Width = 3mm           IV Minimum Solder Mask PCB1 PdbDoc         Advanced PCB         Width Constraint: (0.067mm < 0.254mm) Between Pad Q1-1(41.4mm,16.87mm) on Multi-Layer And Pad Q1-2(41.4mm.15.6mm)           IV Minimum Solder Mask PCB1 PdbDoc         Advanced PCB         Minimum Solder Mask Silver Constraint: (0.067mm < 0.254mm) Between Pad Q1-2(41.4mm.15.6mm) on Multi-Layer And Pad Q1-2(41.4mm.15.4mm)           IV Minimum Solder Mask PCB1 PdbDoc         Advanced PCB         Minimum Solder Mask Silver Constraint: (0.067mm < 0.254mm) Between Pad Q1-2(41.4mm.15.6mm) on Multi-Layer And Pad Q1-2(41.4mm.15.4mm)           Minimum Solder Mask PCB1 PdbDoc         Advanced PCB         Minimum Solder Mask Silver Constraint: (0.067mm < 0.254mm) Between Pad Q1-2(41.4mm.15.6mm)           Minimum Solder Mask	Time 00:22:15 00:22:15 00:22:15 00:22:15 00:22:15 00:22:15 00:22:15	Date 03/04/2018 03/04/2018 03/04/2018 03/04/2018 03/04/2018	No. 1 2 3 4 5 <i>c</i>
Projects • • • • 🗰 Sheet1 SchDoc • 💶 PCB1.PcbDcc • 👔 Design Rule Verification Report			
C, Search			aries
Workspace1.DsnWrk Rule Violations		Count	
BPCB_Project1.PrjPCB     Clearance_Constraint (Gap=0.1mm) (All) (All)		1	
Source occuments     Short-Circuit Constraint (Allowed=No) (All).(All)		1	
Un-Routed Net Constraint ( (All)		0	
Bettings     Modified Polygon (Allow modified: No). (Allow shelved: No)		0	
▲ Documents Width Constraint (Min=0.25mm) (Max=0.5mm) (Preferred=0.254mm) (InNet(GND))		0	_
Chargin Justic Check - Proceed Justic Ch		1	
M Components     Power Plane Connect Rule(Relief Connect V/Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) (Entries=4) (All)		0	_
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)		0	
Hole To Hole Clearance (Gap=0.254mm) (All) (All)		0	
Minimum Solder Mask Sliver (Gap=0.254mm) (All) (All)		4	_
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### OUTPUT



#### Creare un file output-job e salvarlo

Variant Choic <u>e</u>			
This choice of Variant only app	plies to outputs generated fro	om within this view. For release of PCB configurations, variant u	sage is always driven by the
• <b>C</b> +	-1	No Variational	
• Choose a sin	gie variant for the whole o		
Choose a dim	terent variant for each out	put	
If this output	job is used for release of PCB	ang outputs and printing narocopies for neee.	ameter information will be p
		Outputs	
e [	Data Source	Output Description	Enabled
Netlist Outputs			
Simulator Outputs			
IAdd New Simulator Output]			
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Fabrication Outputs			
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Re Report Board Stack			
Composite Drill Guide	•		
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Gerber Files	CB Document]		
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IPC-2581	•		
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Mask Set NC Drill Files ODB++ Files			
Mask Set NC Drill Files ODB++ Files Power-Plane <u>S</u> et			

#### GERBER

		PCB_Project1.PrjPCB	- Altium D	Designer (18.0.9)		
b1	.OutJob *					
			Gerber S	etup		×
	General Layer	rs Drill Drawing Apertures	Advanced			
		Specify the units and format t This controls the units (inches after the decimal point.	o be used in or millimet	n the output files. ers), and the number of digits be	efore and	h1 Outle
2		Units Inches Mijlimeters		Format 4: <u>2</u> 4: <u>3</u> • 4: <u>4</u>		Gene
		The format should be set to s The 4:2 format has a 0.01 mm 0.1 um resolution. If you are using one of the hig manufacturer supports that fo	uit the requ n resolution gher resolut ormat.	irements of your Project. 4:3 has a 1 um resolution, and ions you should check that the F	4:4 has a PCB	Ex

PCB_	Project1.PrjPCB -	Altium Designer (18.0.9)							
Jutiop ^									
Gerber Setup									
	i and a state i a								
General Layers Drill Drawin	ng Apertures A	lavanced							
Layers To Pl	ot	Mechanical Layers(s) to Add to All Plots							
Ex Layer Name	Plot Mirror	Layer Name Pl	ot						
- Top Overlay	×	- Mechanical 1							
- Top Paste		- Mechanical 13							
- Top Solder		- Mechanical 15							
- Top Layer									
- Signal Layer 1									
- Internal Plane 2									
- Rottom Laver									
-Bottom Solder									
-Bottom Paste									
-Bottom Overlay									
-Mechanical 1									
- Mechanical 13									
-Mechanical 15									
-Keep-Out Layer									
- Top Pad Master									
-Bottom Pad Master									
Component Layers									
• Signal Layers									
Electrical Layers									
All Layers									
Plot Lavers T Mirror La		nclude unconnected mid-laver pads							
		ОК	Cancel						

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# Nc drill e pick and place

	NC Drill Se	tup ×						
NC Drill Format			y the choice of var	iants in the PCB configuration				
Specify the units	and format to be used in	the NC Drill output files.						
	units (inches or millimete	ers), and the number of digits before and						
after the decimal	point. Units						PCB_Project1.Prj	PCB - Alt
	Inches		I be passed to this					
	<u>M</u> illimeters	· 4:3						
		• 4: <u>4</u>						Pick ar
The format shoul The 4:2 format h	d be set to suit the requi as a 0.01 mm resolution,	rements of your design. 4:3 has a 1 um resolution, and 4:4 has a 0.1	bled	All Columns	Show	Designator	Comment	
um resolution.				Center-X(mil)		R2	Res1	Top
If you are using o	one of the higher resoluti	ons you should check that the PCB		Center-Y(mil)		R1	Res1	Top
manufacturer sup	oports that format.		/1	Comment		02	MOSEET-N	Top
Leading/Trailing 7	Perces	Coordinate Positions		ComponentKind		01	MOSEET-P	Top
Keep leading	and trailing zeroes	Reference to absolute origin		Description		P4	Header 2	Top
Suppress lead	lina zeroes	Reference to relative origin		Designator		P3	Header 3H	Тор
<ul> <li>Suppress trail</li> </ul>	ing zerges			Footprint		P2	Header 2	Тор
			i i	Footprint Description		P1	Header 2	Тор
Other	anna location commands			Laver				
	errote NC Duil Eles for al	lated \$1 and plated below		Pad-X(mil)				
Generate se	parate IVC Drill files for pi	ated of non-plated noies		Pad-Y(mil)				
Use drilled s	lot command (G85)			Ref-X(mil)				
M Generate Bo	ard Edge <u>Rout</u> Paths			Ref-Y(mil)				
Rout Tool	Dia 2mm			Rotation				
Generate El/	A Binary Drill File (.DRL)			Variation				
				LatestRevisionDate				
		OK Cancel		LatestRevisionNote				
				PackageReference				
				PackageVersion				
				Published				
				Publisher				
				Value				

31/05/2018 d Place Setup AXIAL-0.3 Resistor Resistor 2208.662 Header, 2 Header, 2 Progettazione **Output Settings** Exclude Filter Parameters 25 Include Variation Component Separator -

PCB

#### New FootPrint

<u>F</u> ile	<u>E</u> dit	<u>V</u> iew	Proje <u>c</u> t	<u>P</u> lace	Ľ	<u>esign</u>	Tools	<u>R</u> eports	Wind	ow	<u>H</u> e	lp			
	<u>N</u> ew						Project			۲	1.Pcb	Doc	📴 Job1	.OutJob	6
2	<u>O</u> pen		(	Ctrl+O			<u>S</u> chemat	ic							
	<u>C</u> lose		C	trl+F4		112	<u>P</u> CB						1	0100	8
1	Open	Project.					 Active <u>B</u> C	M Docum	nent			4	2	test 2	8 7
	Open	Desian	Workspa	ce		-	Draftsma	an Docum	ent				4	3	6 5
	Check	Out	- 1			æ	CAM Do	cument				1	~	4	
	Cause			ciul c		-	Output le	ob File						15L62.	36AIRZ-1
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	Run Sc	rint				htr					-				
	itui st	.npt			ļ										

#### Footprint Wizard



#### New Footprint

Attenzione alla griglia:anche se ho scelto Metric ho lo schermo in Inch. Lo cambio con Ctrl +G

9 1	1	<b>&gt;</b>	*						
<u>F</u> ile	<u>E</u> dit	⊻iew	Proje <u>c</u> t	<u>P</u> lace	Tools	<u>R</u> eports	<u>W</u> indow	<u>H</u> elp	
PCB I	Librar	y				<u>C</u> on	nponent		
Mask						Libr	ary List		
					Library Repor <u>t</u>				
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Nor	mal				,	<u>M</u> ea	isure Distar	nce Ctrl+M	
🗸 Select 🔍 Zoom 🗸 Clear Existing						Mea	isure <u>P</u> rimit	tives	



Misurare le distanze : ideale essere sul layer di interesse Per pulire Shift+C

#### **Reference Point**



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#### Associazione con Schematico

Da SCH Library ---properties del componente e poi add



#### Proprietà dei PAD



Nota: attenzione ai fori plated o no

Il nome del PAD deve corrispondere con quello nello chematico

#### Esempio/Esercizio

Realizzare il PCB dello schematico di esempio, realizzando una nuova libreria dei componenti.

